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Automated Fault Diagnosis in Digital VLSI Circuits via Deep Learning Models

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ABSTRACT

Finding and resolving faults in integrated circuit design has become an increasingly important phase as the complexity of digital VLSI circuits continues to increase. A novel deep learning (DL) defect detection model that makes use of an artificial neural network (ANN) known as stacked sparse autoencoder (SSAE) is going to be developed to fulfill the objectives of this study. This strategy, which intends to handle the issue in the exploration field, has as its major goal the use of SSAE for the purpose of detecting abnormalities and identifying features in vast electrical circuits. The creation of test patterns, the reduction of characteristics, and the identification of flaws are the three primary phases that comprise the model. Over the course of the SSAE phase, unsupervised learning using training data is used in order to enhance the process of feature extraction. As part of the process of evaluating the success of feature extraction, the architecture of the SSAE network may include certain modifications. A 99.7 percent reduction in features is achieved with the use of SSAE for test patterns, and a 99.3 percent fault coverage is achieved through the utilization of ATALANTA.

Index Terms **- Automatic Test Pattern Generation, ANN, Fault Detection, Digital Circuit, ML, SSAE, Test Pattern.**

INTRODUCTION

As the world of digital technologies continues to evolve at a rapid pace, the significance of computer-based system authentication, fault identification, and repair methods has soared. When it comes to large and complex digital systems, fault detection becomes a serious problem due to the sheer complexity of the circuits and the availability of a wide variety of design flaws [2]. The use of artificial intelligence (AI) to enhance the effectiveness of defect detection has been the focus of research activities that are now being undertaken as a solution to these issues [3]. Highlighting the complexity of these phases is the large contribution [4] that debugging and correction make in the stages of integrated circuit (IC) design. These stages account for an average of 70 percent of the total time spent on the design. The creation of quick algorithms for repairing and debugging that adhere to behavioral requirements was the primary focus of efforts made in order to reduce the amount of time and money spent. The study investigates how machine learning systems may effectively detect issues that are stuck at a certain point in time by using a range of datasets that have been acquired via test pattern generators. Another area that is discussed is the use of SAT-based algorithms [5] to identify errors that occur while replacing gates. The significance of the dataset in machine learning models is brought to light by digital Very Large-Scale Integration (VLSI) circuits, which make use of the results generated by test pattern generators.

We will examine the effectiveness, flexibility, and fault coverage capabilities of a variety of high-tech Automatic Test Pattern Generation systems [6], one of which is the ATALANTA software, which was developed at Virginia Tech University and is quite inexpensive. Some earlier methods of doing things are compared to more contemporary methods that make use of deep learning techniques, such as artificial neural networks (ANNs), to improve mistake detection and correction. Research is being conducted to determine whether or whether the SAT and MAX-SAT algorithms are useful tools for locating and correcting specific errors, such as replacing gates. By using advanced SAT solvers and breaking the process down into Boolean satisfiability questions, we are able to illustrate how effectively these tools are able to discover specific facts and attributes of fault instances. An strategy that is based on DL was proposed by the current study as a means of effectively identifying features and detecting defects in combinational digital circuits. Stacking sparse autoencoders were used in the study project in order to correctly compress massive amounts of data and return essential properties. Following the presentation of deep learning (DL) and autoencoders, the subsequent sections must include a comprehensive description of the model's requirements, an evaluation of its performance, and, lastly, a conclusion.

LITERATURE REVIEW

Moness et al. [7] presented a novel semi-supervised Fault Detection (FD) model for combinational and sequential circuits. This model was developed with the help of Deep Sparse Autoencoder. It outperforms conventional machine learning models, boasting a maximum validation accuracy of 99.93% for combinational circuits and 99.95% for sequential circuits, respectively, with a running time that is 187 times faster than approaches based on SAT solvers. The greatest validation accuracy that it obtains is 97.8%, which is higher than the accuracy of FD models that are based on Radial Basis Function Network (RBFN). Dependencies on datasets and the need for more comprehensive circuit testing are also examples of constraints. An approach to defect identification in analog circuits was published by Shokrolahi et al. [8] in the form of a deep Convolutional Neural Network (CNN) that was fed images of Power Spectrum Density (PSD). The PSD-CNN methodology that was recommended achieves an accuracy of 99.8 percent, which is a considerable improvement over the approaches that were previously used. The need for a wide variety of datasets is one possible constraint, which may restrict its use to certain types of circuits for which it is most beneficial.

[9] Khalil et al. provided an early approach for forecasting transistor defects by using FFT, PCA, and CNN. This method was early in its development. An incredible 98.93% accuracy is achieved when it is used to 45nm technology circuits, which is a significant improvement over the state-of-the-art techniques. There are potential limitations, such as applications that are circuit-specific. In this technique, frequency domain fault signs are extracted, dimensions are reduced, and finally, final features are presented and classified. This technology is a combination of FFT, PCA, and CNN. The recommended method outperforms other techniques that are currently in use, with an accuracy of failure prediction that is 98.93% higher than anything else. Because the power consumption of implementing hardware on an Altera Arria 10 GX FPGA is just 1.08 W, this is obviously something that can be accomplished.

A system that takes use of machine learning methods that are based on MATLAB was presented by Arabi et al. [10] in order to identify and categorize certain parametric circuit defects. Through the use of Orcad PSpice for data collection and Monte Carlo analysis for simulation, the technique is able to attain an outstanding level of accuracy. In the first circuit, it functions flawlessly; in the second circuit, it achieves a score of 99.77%; and in the third circuit, it achieves a score of 99.72%. Both the dependence on the accuracy of the simulation and the presence of certain types of errors are examples of possible constraints. When everything is taken into consideration, the classification method that has been provided is more effective than the research that have been done in the past on the topic of defect detection and classification.

In their study [11], Hussein and colleagues presented a DL-based semi-supervised Fault Detection (FD) model that was designed for sequential and combinational circuits. This model exhibits the effectiveness of employing deep learning for fault diagnosis in digital circuits. It outperforms typical machine learning models and techniques based on SAT solvers, with validation accuracy of 99.93% for combinational circuits and 99.95% for sequential circuits, respectively. In a research that was conducted by Gaber and colleagues [12], the authors explored how the complexity of digital VLSI circuits might have an effect on verification methods. By recommending an incremental correction approach, it is possible to reduce the amount of dependence on specialized patterns while also providing compact test patterns. It is possible that one of the limits is contingent upon certain circuits.

For the purpose of addressing the challenges associated with fault identification in Through Silicon Vias (TSVs), Radhakrishnan et al. [13] proposed an Efficient Partitioning and Placement-based Fault TSV detection in three-dimensional integrated circuits. It's possible that some limits are related to the requirements for maximum efficiency. An LSTM model was provided by Wang et al. [14] in order to facilitate the most effective identification of intermittent issues in electronic systems that are accessible online. Both the model's high recall (87 percent accuracy) and its precision (97 percent accuracy) are evidence of its effectiveness. It is possible that there are instances that are optimal in terms of performance. This is one constraint.

METHODOLOGY

Autoencoders

Through the use of an autoencoder (AE), a strong unsupervised machine learning approach, it is feasible to reduce the dimensions from high to low. It takes an input, compresses it into a latent space, and then decodes it, retaining just the features that are most significant while deleting the remainder of the characteristics. Before supervised algorithms, such as classifiers, to make effective use of encoded data, the decoder must first reconstruct input from the encoding. This is necessary in order for the algorithms to succeed. One example of an AE process may be seen in Figure 1, which you can view.Minimal auto encoders.

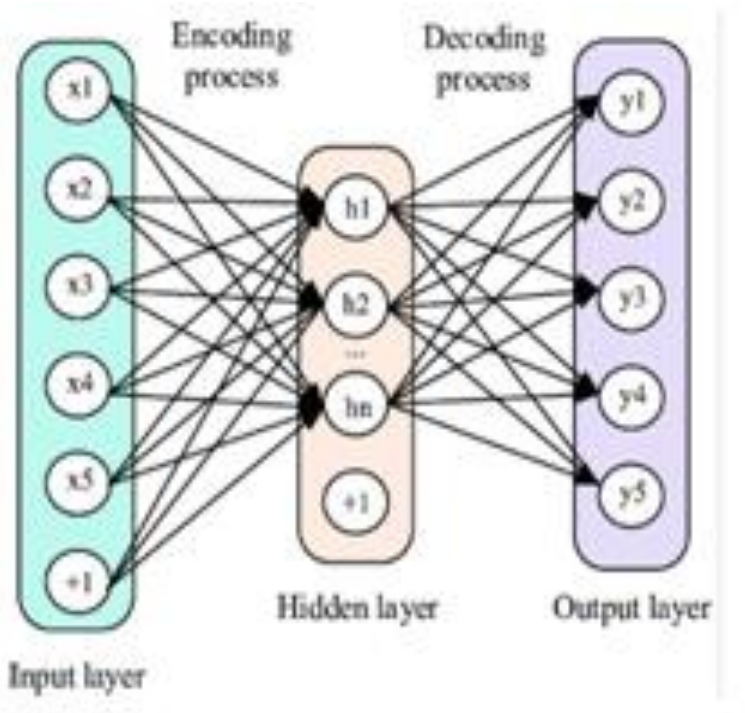


Fig.1: Procedure for auto encoder

Rather of creating a bottleneck without reducing the number of nodes in the hidden layer, sparse autoencoders (SAE) attempt to maintain the number of nodes in the hidden layer by activating a limited number of neurons. This is accomplished via the use of a sparsity criterion and a loss function that penalizes the activation of hidden layers. Figure 2 depicts a sparse autoencoder for your viewing pleasure.

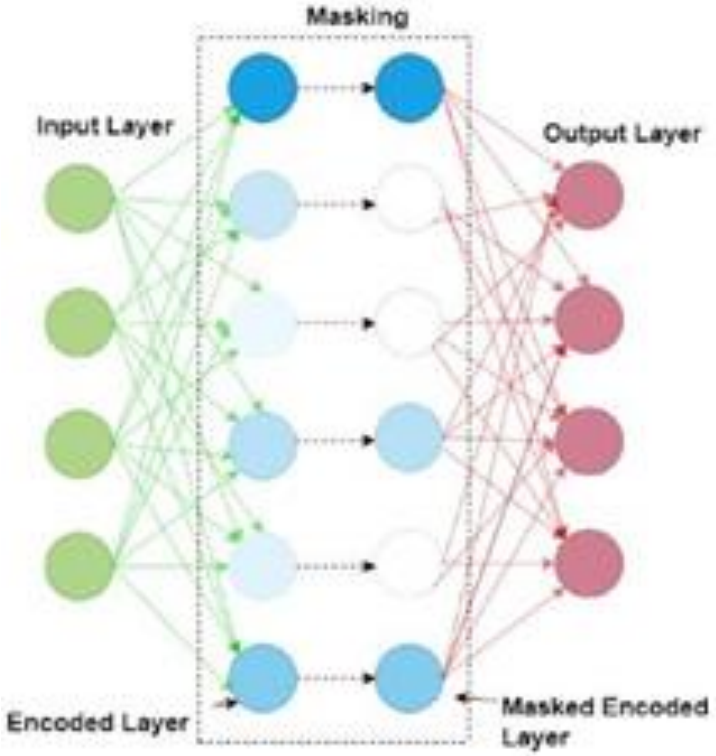


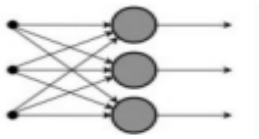
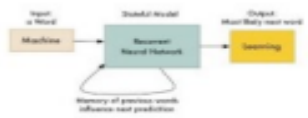
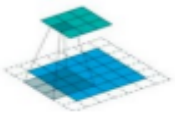
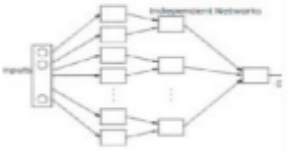
Fig.2: Compact autoencoder

Deep learning

DL is a technique that is both effective and considered to be state-of-the-art when it comes to the automated extraction of features and the identification of problems. By making use of large datasets and using deep learning to identify essential features, it is possible to obtain improved fault detection performance in comparison to more conventional methods. There are many different kinds of neural networks (NN), and the following table gives a comparison of them:

Table1: Evaluate NNs

SSAE

Classification of deep NN	Description	Applications	Visual representation
Feedforward NN	- Basic configurations of artificial neural networks (ANN). - Input data flows unidirectionally from input nodes to output nodes. - It may include hidden layers or not. - Backpropagation is absent, often utilizing a classifying activation function. - Operates with a front-propagated wave.	Categorization involving intricate target classes.	
Recurrent NN	- Records the output and loops it back to the input for accurate predictions. - Each neuron functions akin to a memory cell. - The learning rate is employed to determine the accurate prediction.	- Models for converting text to speech (TTS).	
Convolution NN	- Resembles a feedforward neural network. - Input features are processed in batches.	Applicable in the realm of image processing and computer vision.	
Modular NN	- Comprising several independent networks. - Inputs for each neural network differ, facilitating distinct sub-tasks without interaction. - Breaking down extensive processes into smaller models to reduce complexity. -Processing time is contingent on the quantity of neurons.	- Numerous applications like approximating functions, recognizing characters, and developing a patient -independent ECG recognition system.	

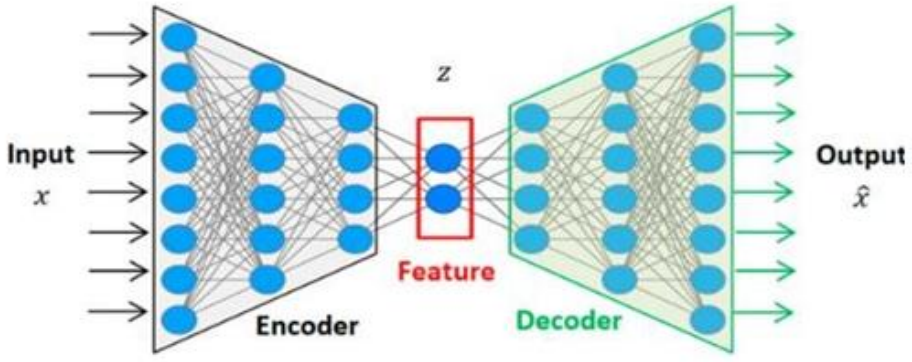


Fig3: DeepAE

When dealing with complex structures, SSAE or Deep AE is used in order to enhance the efficiency that is distinctive of AE. This autoencoder, which has multiple layers that are layered on top of one another, receives data from one encoder layer and utilizes it to train the following encoder layer. Following the completion of two independent stages of unsupervised training, the network moves onto a supervised stage. Figure 3 is an illustration of a deep autoencoder that you may find interesting.

Discovering Defects using DL

Stacked SSAE eliminates the need for accurate mathematical models or formal specifications when it comes to the process of locating flaws in digital VLSI circuits. In order to compress data, SSAE makes use of unsupervised learning, which is made possible with the assistance of test vectors generated by the powerful ATPG tool ATALANTA. A normalized probability distribution is produced by the final softmax layer, which plays a role in classification via the use of the softmax function and enables clear interpretation. In the multi-category classifier, the k-th number of categories, the zi-th output vector of the neural network, and the z-th input vector of the softmax are all important variables.

Proposed Approach of Identifying Abnormalities

Approach to Identifying Abnormalities That Is A Proposed Method

Step1:TestPatternGeneration

First and foremost, the process involves the development of comprehensive and one-of-a-kind test patterns for the digital circuit. Through the use of the ATALANTA tool, which is based on the FAN algorithm, it is possible to construct many sequences that have been evaluated, each of which has its own unique collection of right results and abnormalities masks.

Step2: Feature Reduction

Unsupervised learning with SSAE is carried out by the neural network after the creation of data, which is an essential step in the process of reducing the feature dimensions in large digital circuits. In order to get the fewest features without compromising accuracy, the goal is to train on test patterns and responses without making any mistakes. The effective distillation of pertinent information that SSAE provides contributes to an overall improvement in performance, particularly in the area of fault identification.

Step3:Fault Detection

In conclusion, a softmax classifier is used in order to enumerate mistakes for each and every test pattern. The classifier transforms the real data into probabilities in order to increase the overall effectiveness of the system and to make it easier to distinguish between different types of problems.

RESULTS AND DISCUSSION

The approach makes use of an SSAE in order to identify stuck-at-0 and stuck-at-1 errors on eight integrated circuits by using the technique. In order to do this calculation, procedures that were first designed for the ISCAS'85 standard are used. The software was powered by an Intel Core i7 10750 processor operating at 2.6 GHz and 16 gigabytes of random access memory (RAM) during its whole. In order to do this, we used the ATALANTA tool to conduct an analysis on each ISCAS'85. To be more exact, we generated a particular number of test patterns for each kind of mistake, including one that was stuck at 0 and one that was stalled at 1. At the end of the day, thirty-one out of fifty test vectors were selected for the purpose of identifying defects in digital circuits. The information on the electrical circuits is shown in Table 2, which includes the inputs and outputs of the circuits, test vectors, fault coverage percentage, and defect count.

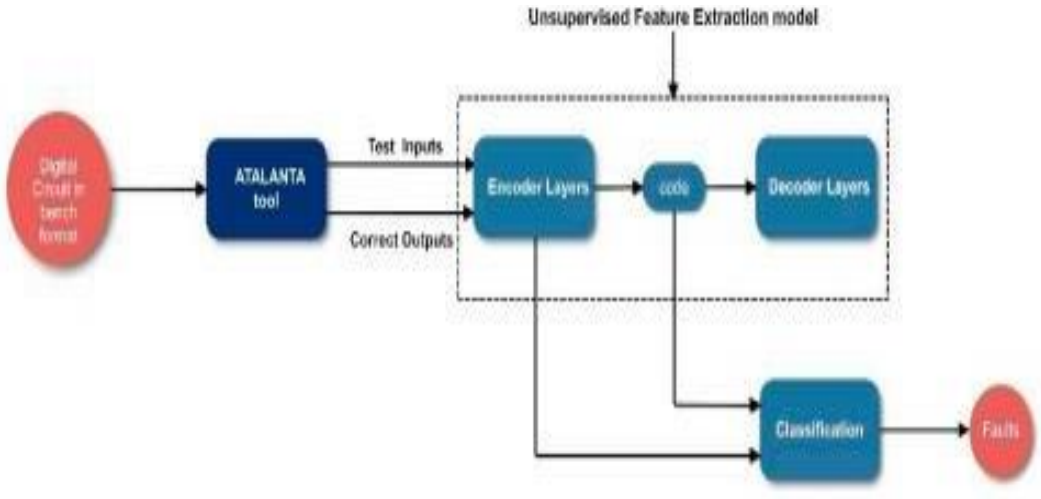


Fig4: proposed model

Table2: Quantity of inputs and outputs, test patterns, fault coverage, and number of occurrences for eight combinational circuits.

CNF Type	Inputs and outputs quantity	fault occurrences	test patterns	Fault Coverage
c17	7	22	54	100%
c432	43	524	8950	98.8%
c499	73	758	13066	95.5%
c880	86	942	45356	100%
c1908	58	1879	34216	99.2%
c3540	72	3428	55752	95.9%
c5315	301	5350	88978	98.7%
c6288	64	7744	114101	80.8%

There is a complete listing of all of the SSAE parameters in Table 3. Through the use of experimental adjustments, the optimal feature reduction was accomplished. In addition, in order to improve the efficiency of the SSAE reconstruction, the sparsity constraint (ﻩ) was experimentally fine-tuned. This was done with the batch size of 32 and 100 epochs in mind. Moreover, the table presents a comparison between the validation accuracy of basic AE and that of SSAE verification. When we compare the two, we can see that the "c5315" circuit, which initially had 300 inputs and outputs but was reduced to 21 by employing three SSAE with a sparsity of around 10e-9, achieves a peak reconstruction accuracy of approximately 99.7 percent. This is because the sparsity of the circuit was reduced to 21.

Table3:Validation accuracy and the amount of hidden neurons in feature extraction under sparsity restrictions.

CNF Type	Quantity of hidden neurons	Validation Accuracy using simple AE	Validation Accuracy using SSAE	Sparsity Constraints of SSAE
c17	5,3,2	63.9%	71.4%	10e-3
c432	30,20,10	95.4%	97.5%	10e-6
c499	50,30,20	98.2%	98.50%	10.e-9
c880	50,30,20	98.3%	98.6%	10e
c1908	50,30,20	97.8%	98.8%	10e
c3540	50,30,20	97.3%	98.2%	10e
c5315	100,50,20	98.9%	99.7%	10.e-9
c6288	50,30,20	97.9%	99.3%	10e-6

There is a correlation between the sparsity constraint (ρ) and the accuracy of the SSAE, as seen in Figure 9. In this study, five different combinational circuits were evaluated using a range of sparse restrictions, including $\rho\rho_1$=0.50, $\rho\rho_2$=0.067, and $\rho\rho_3$=0.024. For the construction of the SSAE model, three Sparse Autoencoders (SAE) were used in accordance with the design shown in Table 3. According to the data, the optimal value for sparsity restrictions is somewhere around 0.024 as the sweet spot.

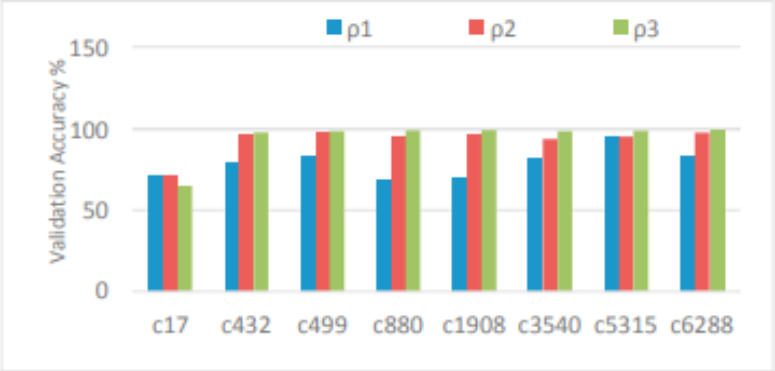


Fig.5: Effects of sparsity limits on SSAE accuracy

CONCLUSION

An unique artificial neural network (ANN)-based technique was proposed in the research for the purpose of identifying stuck-at-faults in the 27-channel interrupt controller and Arithmetic Logic Units circuits that were derived from the ISCAS'85 benchmarks. Through the exploitation of test patterns that are created by the ATALANTA program, the algorithm is able to handle the difficulty of search space explosion. This is accomplished by compressing digital circuit characteristics. The use of a stack consisting of three sparse AEs improves the algorithm's capability to reach optimum reconstruction accuracy, which is very advantageous when it comes to the diagnosis and repair of extensive-scale electronic circuits. By using fault masks, SSAE is included into a softmax classifier for the purpose of supervised learning integration. When applied to eight logical circuits, the method achieves a fantastic fault coverage of roughly 99.3% with ATALANTA, while at the same time attaining approximately 99.7% using test patterns.

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