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The Groundsmen of the Semiconductor Industry: Leadership where Necessary, Infrastructure were Essential

Lahar Alok Agrawal

UG Student, Department of CCE, Manipal University, Jaipur, Rajasthan

ABSTRACT

The responsibilities of the stakeholders can be easily decided but the responsibilities of the Stake creators must be defined. TheGamet of Responsibilities are also now the challenges of this Industry. They are understanding that they are the grounds men of the industry and not the players of the industry. They are getting 'Leadership where Necessary, Infrastructure were Essential. In this research, a theoretical overview on semiconductor industry has been described along with its other important concerns over policies and frameworks.

INTRODUCTION

The 'Quad Supply Chain Initiative' announced at the first in-person summit of the group, can be expanded to include trade secret protections that will facilitatetechnology transfer agreements easily[2]. India can start by introducing and ensuring the enforcement of strict rules against IP theft and other regulations in the semiconductor industry [3]. This always become a persuasive argument by the criticizers of Indian Trade Policy.Semiconductor Integrated Circuits Layout-Design Registry (SICLDR) is the office where the applications on Layout-Designs of integrated circuits are filed for registration of created IPR. The jurisdiction of this Registry is whole of India. The Registry, as per the guidelines laid down in the Semiconductor Integrated Circuits Layout Design (SICLD) Act 2000 and the Semiconductor Integrated Circuits Layout-Design (SICLD) Rules 2001, examines the layout-designs of the Integrated Circuits and issues the Registration Certificate to the original layout-designs of the Semiconductor Integrated Circuits [4]. The Act affords protection to the layout-design of a semiconductor integrated circuit. Protection is given to the layout-design itself so that design houses producing layout-designs would have protection for those products separate from their incorporation in a chip product[5].India is a member of the TRIPS Agreement which itself obliges adherence to **Article 2** through 7 of the IPIC Treaty [6]. "Holder of the right" means the natural person who, or the legal entity which, according to the applicable law, is to be regarded as the beneficiary of the protection referred to in Article 6, IPIC Treaty [7].

System Reforms

a) Palette of Scheme

In furtherance of the vision of Aatmanirbhar Bharat and positioning India as the global hub for ESDM, a comprehensive program for the development of semiconductors and display manufacturing ecosystem in India was approved by Government of India with an outlay of ₹ 76,000 crore (>10 billion USD). The Programme contained various schemes to attract investments in the field of semiconductors and display manufacturing. The Union Cabinet in its meeting held on 21.09.2022 has accorded its approval for modification of this programme. Following modifications have been approved. Fiscal support of 50% of Project Cost on pari-passu basis for all technology nodes under Scheme for Setting up of Semiconductor Fabs in India.Fiscal support of 50% of Project Cost on pari-passu basis under Scheme for Setting up of Display Fabs.Fiscal support of 50% of Capital Expenditure on pari-passu basis under Scheme for Setting up of Compound Semiconductors / Silicon Photonics / Sensors Fab and Semiconductor ATMP /OSAT facilities in India. Additionally, target technologies under the Scheme will include Discrete Semiconductor Fabs.The programme aims to provide attractive incentive support to companies / consortia that are engaged in Silicon Semiconductor Fabs, Display Fabs, Compound Semiconductors / Silicon Photonics / Sensors (including MEMS) Fabs / Discrete Semiconductor Fabs, Semiconductor Packaging (ATMP / OSAT) and Semiconductor Design [8].

b) Semiconductor Fabs and Display Fabs

The Modified Schemes for Setting up of Semiconductor Fabs and Display Fabs in India shall extend fiscal support of 50% of project cost on pari-passu basis to applicants who are found eligible and have the technology as well as capacity to execute such highly capital and resource intensive projects. Government of India will work closely with the State Governments to establish High-Tech Clusters with requisite infrastructure in terms of land, semiconductor grade water, high quality power, logistics and research ecosystem to approve applications for setting up at least two greenfield Semiconductor Fabs and two Display Fabs in the country [9].

c) Compound Semiconductors / Silicon Photonics / Sensors (including MEMS) Fabs/ Discrete Semiconductor Fabs and Semiconductor ATMP / OSAT Units

The Modified Scheme for Setting up of Compound Semiconductors / Silicon Photonics / Sensors (including MEMS) Fabs / Discrete Semiconductor Fabs and Semiconductor ATMP / OSAT facilities in India shall extend fiscal support of 50% of capital expenditure on pari-passu basis to applicants who are found eligible and have the technology to execute such projects. At least 20 such units of Compound Semiconductors and Semiconductor Packaging are expected to be established with Government support under this scheme [10].

d) Semiconductor Design Companies

The Design Linked Incentive (DLI) Scheme shall extend product design linked incentive of up to 50% of eligible expenditure and product deployment linked incentive of 6% - 4% on net sales for five years. Support will be provided to 100 domestic companies of semiconductor design for Integrated Circuits (ICs), Chipsets, System on Chips (SoCs), Systems & IP Cores and semiconductor linked design and facilitating the growth of not less than 20 such companies which can achieve turnover of more than Rs.1500 crore in the coming five years[11].

e) Semi-conductor Laboratory (SCL)

Union Cabinet has also approved that Ministry of Electronics and Information Technology will take requisite steps for modernization and commercialization of Semi-conductor Laboratory (SCL), Mohali. MeitY will explore the possibility for the Joint Venture of SCL with a commercial fab partner to modernize the brownfield fab facility [12].

f) India Semiconductor Mission

In order to drive the long-term strategies for developing a sustainable semiconductors and display ecosystem, a specialized and independent "India Semiconductor Mission (ISM)" has been set up. The India Semiconductor Mission will be led by global experts in semiconductor and display industry. It will act as the nodal agency for efficient and smooth implementation of the schemes for setting up of Semiconductor and Display Fabs[13].

g) System becoming a Support System

The system, which has always been known for squeezing the applications which always got stuck between big files, is trying to create a research friendly environment.

IIT Bombay: India has developed academic R&D in semiconductors through the Centers of Excellence in Nanoelectronics (CENs), where IIT Bombay is a pioneering institution [14].A key deliverable of the semiconductor ecosystem building led by the Minister is to establish Silicon manufacturing and innovation ecosystem. Hence, the first indigenous memory developed on a 180 nm CMOS technology platform depicted a significant occasion in this techade. The 8-inch wafer containing the pioneering one-time programmable (OTP) memory translated from IITB Lab to SCL Fab for productization [15].

IISc: The Centre for Nano Science and Engineering (CeNSE) was established in 2010 to pursue interdisciplinary research across several disciplines with a focus on nanoscale systems. Current research topics include, but are not limited to nanoelectronics, MEMS/NEMS, nanomaterials and devices, photonics, nano-biotechnology, solar cells and computational nano-engineering.

*Gallium Nitride (GaN) transistors for power and RF applications:Due to unique material properties such as high polarization, wide band gap, high carrier mobility and velocity, Gallium Nitride and its alloys (III-nitride family) have enabled transistors with much superior performance compared to traditional silicon devices in the areas of high-power switching and RF power amplification.

*Nanotechnology is all about scaling down the size of devices: The logical extreme of this effort are low-dimensional semiconductors whose critical dimension is only one or few atoms thick. 1D semiconductors like carbon nanotube and

2D semiconductors like graphene, belong to this class of materials. CeNSE has a very successful program to deposit these exciting materials over large areas for various applications [16].

IESA:IESA is the premier industry body representing the Indian Electronic System Design and Manufacturing ESDM industry and has represented it since 2005. It has close to 300 members - both domestic and multinational enterprises. IESA is committed towards building global awareness for the Indian ESDM industry and supporting its growth through focused initiatives in developing the ecosystem. This is through publishing credible data, networking events and alliances with other international associations. IESA works closely with the Government as a knowledge partner on the sector, both at the centre and at the state level [17].

AICTE: AICTE have designed two courses namely

1. BTech Electronics (VLSI Design and Technology)**,**
2. Diploma in IC manufacturing

Policy Intent

Setting up of ATMP Plant: Setting up of ATMP plant by an Integrated Device Manufacturer like MicronTecnologies in the Memory Category is the best kickstart which could have happened. Memory is better to start with as it constitutes>30% of the Semiconductor Manufacturing and variety is limited [18].

Foundry Fab: Company like Vedanta procured a license for "Protection grade technology for 40nm from a prominent IDM" [19]. They will shortly acquire a license for production grade 28 nm as well.

Taiwanese Collaborations: An electronics Assembly Company Foxconn may partner with TSMC and TMH. They are looking up to 4-5 lines of Fabs [20].

External Research and Training: Lam Research Labs will train 60,000 engineers on the Semi verse Platforms about Semiconductor technologies.

Components Manufacturing: An American Company Applied Materials will manufacture and design complex equipment in India.

Memorandum of Understanding [U.S.A]:A Memorandum of Understanding (MoU) on establishing semiconductor supply chain and innovation partnership under the framework of India – US Commercial Dialogue was signed between the two countries following the Commercial Dialogue 2023 held in New Delhi today.The MoU seeks to establish a collaborative mechanism between the two governments on Semiconductor Supply chain resiliency and diversification in view of US's CHIPS and Science Act and India's Semiconductor Mission.The MoU seeks to establish a collaborative mechanism between the two governments on Semiconductor Supply chain resiliency and diversification in view of US's CHIPS and Science Act and India's Semiconductor Mission [21].

Memorandum of Cooperation [Japan]: The MoC will help to promote the movement of skilled workers from India to Japan. The MoC covers 14 categories of specified skills under which skilled workers from India who meet the skills requirement and Japanese language tests would be eligible for employment in Japan on a contractual basis. The 14 specified industry fields include nursing care, building cleaning, material processing, industrial machinery manufacturing, electric and electronic information, construction, shipbuilding and ship-related industry, automobile maintenance, aviation, lodging, agriculture, fisheries, food and beverages manufacturing and food services industry. Japan would grant these workers the status of "specified skilled worker". It is also expected that Indian skilled workers who go to Japan under this MoC will acquire new skills while working in Japan. A Joint Working Group (JWG), comprising officials from both countries, will be constituted in the near future to work out operational details and smooth implementation of this programme [22].

Aim of the Ministry

* 2 ATMP/OSAT units Ecosystem in the Next 3 years.
* 2 Compound Semiconductors (GaN, SiC) fabs in the next 4 years.
* 2 silicon fabs in the next 5 years [23].

CONCLUSION

The industry which was not even discussed about in the mainstream media few years before, on which issue a report published by Indian Semiconductor Association supported by Department of Information Technology, prepared by

Ernst & Young called the phase as 'Innovation Phase' and stated "Another reason for high attrition can be attributed to high recruitment by large third-party service providers, who were traditionally in the enterprise application space " and "the countries mentioned above (China, Taiwan, Southeast Asia) have had a complete and mature ecosystem which has been built over the past 30 years "[24] . This shows that from struggling between the void of opportunities and talent to aiming for becoming a major player in the Chip Diplomacy. This journey justifies giving "OK and Check" remark for the pitch created by thegroundsmen, but must manage the matches, maintain the pitch, and build an academy. Not stopping is the only way to go further.

REFERENCES

[1]. Shri Sanjeev Sanyal, Member, EAC to the Prime Minister of India
[2]. Harnessing trade policy to build India's semiconductor industry, By Pranay Kotasthane and Arjun Gargeyas.
[3]. Harnessing trade policy to build India's semiconductor industry,By Pranay Kotasthane and Arjun Gargeyas.
[4]. SICLDR, Government of India.
[5]. Rights under the Semiconductor Act, 2000, 17 December 2014.
[6]. IPIC Treaty, World Trade Organization.
[7]. MeitY, Government of India.
[8]. MeitY, Government of India.
[9]. MeitY, Government of India.
[10]. MeitY, Government of India.
[11]. MeitY Government of India.
[12]. MeitY, Government of India.
[13]. MeitY, Government of India.
[14]. CENs, IIT Bombay.
[15]. Shri Rajeev Chandrashekhar,MoS,MeitY, Government of India.
[16]. CeNSE, IISc Bengaluru.
[17]. IESA.
[18]. Dr. Satya Gupta, VLSI Society of India.
[19]. MeitY, Government of India.
[20]. MeitY, Government of India.
[21]. MEA, Government of India.
[22]. MEA, Government of India.
[23]. Shri Ashwini Vaishnaw, Cabinet Minister, MEITy, Government of India.
[24]. MeitY, Government of India