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Design and Appraisal of a High-Efficiency CMOS 18nm NAND-Based SR Latch For Expedited and Low-Power Digital Applications

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ABSTRACT

A Sense-Amplifier-based Flip-Flop (SAFF) suitable for low-power high-speed operation. With the employment of a new sense-amplifier stage as well as a new single-ended latch stage, the power and delay of the flip-flop is greatly reduced. The proposed SAFF can provide low voltage operation by adopting Multi Threshold Complementary Metal Oxide Semiconductor (MTCMOS) optimization. The proposed SAFF delay and the power are smaller than those of the existing Master-Slave Flip- Flop (MSFF). The power-delay-product of the proposed SAFF improves compared with the conventional SAFF and MSFF, respectively the area of the proposed flip-flop decrease, the proposed SAFF could provide robust operation even low power supply voltages. But in this design, we are using 45nm technology by using this technology we can get the required output by giving 1LVT (Low Threshold Voltage).

Keywords: Sense-Amplifier-Based Flip-Flop, Low-Voltage Operation, MTCMOS, Power-Delay Product, Dynamic Latch, 45 nm CMOS, High-Speed Digital Design.

INTRODUCTION

The continuous scaling of CMOS technology has enabled the integration of billions of transistors on a single chip, leading to highly complex and high-performance digital systems [1]. As technology scales into deep submicron regions such as 45 nm and below, power consumption and propagation delay have become critical design challenges [2]. In synchronous digital circuits, flip-flops are widely used as storage elements and are fundamental components in registers, counters, pipelines, and finite state machines [3]. Since flip-flops are triggered by the clock signal, they contribute significantly to overall power dissipation, particularly clock-related dynamic power [4]. Consequently, optimizing flip-flop architectures is essential to improve system speed and reduce energy consumption [5].

Traditionally, the Master–Slave Flip-Flop (MSFF) has been widely adopted in digital designs due to its robustness and simplicity [6]. The MSFF consists of two cascaded latches controlled by complementary clock signals. Although reliable, this structure suffers from relatively large setup time and clock-to-Q delay because data must propagate through multiple stages before being latched [7]. Furthermore, the large number of transistors and clocked devices increases dynamic power consumption and clock loading [8]. As clock frequency increases in modern processors and communication systems, these limitations become more pronounced [9].

To overcome the limitations of MSFF, pulse-triggered flip-flops (PFFs) were introduced as a high-speed alternative [10]. PFFs employ a single latch controlled by a short clock pulse, enabling near-zero setup time and reduced delay [11]. However, the performance of PFFs strongly depends on accurate pulse-width generation [12]. If the pulse width is too narrow, data capture may fail; if too wide, hold time increases and power consumption rises [13]. Variations in process, voltage, and temperature (PVT) further complicate reliable pulse generation [14]. These challenges restrict the practical application of PFFs in robust designs [15].

The Sense-Amplifier-Based Flip-Flop (SAFF) emerged as an effective solution for high-speed applications [16]. Originally derived from sense-amplifier circuits used in memory read operations, the SAFF combines a sense-amplifier stage with a latch stage [17]. The sense-amplifier rapidly detects small input voltage differences and amplifies them to full logic levels,

enabling fast data capture immediately after the clock transition [18]. As a result, SAFFs achieve near-zero or even negative setup time, making them suitable for high-frequency pipeline architectures [19].

Despite their speed advantage, conventional SAFFs exhibit certain drawbacks [20]. The pre-charge operation required in the sense-amplifier stage increases dynamic power consumption [21]. Additionally, conventional latch designs may introduce glitches or unnecessary switching activity, further increasing power dissipation [22]. Another critical concern in scaled technologies is leakage current, which becomes significant at lower threshold voltages [23]. As supply voltage is reduced to minimize dynamic power, ensuring reliable low-voltage operation becomes increasingly challenging [24].

To address leakage and low-voltage reliability issues, Multi-Threshold CMOS (MTCMOS) techniques have been proposed [25]. MTCMOS utilizes transistors with different threshold voltages within the same design to balance speed and leakage power [26]. Low Threshold Voltage (LVT) devices are used in critical paths to maintain high performance, while High Threshold Voltage (HVT) devices reduce leakage in non-critical paths [27]. This technique is particularly effective in flip-flop design, where both speed and leakage optimization are required [28].

In this work, a low-power, high-speed SAFF architecture implemented in 45 nm CMOS technology is proposed [29]. The design introduces a modified sense-amplifier stage with reduced pre-charge capacitance and an optimized single-ended latch structure to minimize switching activity and delay [30]. Furthermore, MTCMOS optimization is integrated to achieve robust operation under reduced supply voltage conditions. By combining architectural improvements with threshold voltage engineering, the proposed flip-flop achieves lower delay, reduced power consumption, improved power-delay product, and smaller area compared to conventional MSFF and SAFF designs.

LITERATURE SURVEY

The evolution of flip-flop design has been closely linked to the scaling of CMOS technology and the increasing demand for high-speed, low-power digital systems. Alioto et al. [1] conducted a comprehensive analysis of energy–delay trade-offs in nanometre CMOS flip-flops, establishing that storage elements significantly influence overall system efficiency. Chan and Sachdev [2] further explored low-power flip-flop implementations in 65-nm CMOS, demonstrating that transistor sizing and clock load reduction are critical for minimizing dynamic power. He and Sinencio [3] proposed a high-performance flip-flop in 90-nm CMOS, achieving improved timing characteristics through optimized device selection and layout techniques. To address timing challenges in scaled technologies, Jeong et al. [4] introduced a low-voltage pulsed latch with reduced hold time, enabling reliable high-frequency operation. Kim et al. [5] presented a high-speed sense-amplifier-based flip-flop (SAFF), highlighting the advantage of differential sensing for near-zero setup time. Lin and Hwang [6] proposed a single-ended SAFF structure focused on reducing power consumption while maintaining speed performance. Earlier, Matsui et al. [7] demonstrated the practical application of sense-amplifying flip-flops in a 200-MHz pipelined CMOS datapath, confirming their suitability for high-speed architectures. Montanaro et al. [8] validated these concepts in a 160-MHz RISC microprocessor, proving that optimized clocked storage elements significantly enhance processor performance.

Nikolic et al. [9] improved SAFF robustness and minimized clock-to-Q delay through refined transistor-level design. Oklobdzija [10] provided a detailed comparison of clocked storage elements, including master–slave, pulsed, and sense-amplifier-based flip-flops, emphasizing performance and energy considerations. Pan and Chen [11] introduced a conditional feed-through pulsed flip-flop to enhance speed while controlling switching activity. Partovi et al. [12] explored hybrid latch and edge-triggered flip-flop elements to balance performance and clock loading. Sakurai and Newton [13] developed the alpha-power law MOSFET model, enabling accurate delay prediction in deep submicron CMOS circuits. Suzuki et al. [14] earlier investigated clocked CMOS circuitry, laying the groundwork for synchronous storage design.

Teh et al. [15] proposed a conditional capture flip-flop to reduce unnecessary transitions and dynamic power consumption. Veendrick [16] analyzed short-circuit power dissipation in static CMOS circuits, identifying switching overlap currents as a major contributor to power loss. Weste and Harris [17] provided comprehensive CMOS VLSI design principles, including timing constraints and clocking methodologies relevant to flip-flop optimization. Rabaey et al. [18] emphasized energy-efficient digital integrated circuit design, particularly focusing on minimizing clock power. Kang and Leblebici [19] elaborated on CMOS digital circuit analysis and timing issues affecting latch and flip-flop reliability.

Chandrakasan et al. [20] introduced system-level low-power CMOS design strategies, integrating architectural and circuit-level optimizations. Roy et al. [21] examined leakage current mechanisms in nanometer technologies, highlighting the growing significance of subthreshold and gate leakage in flip-flop circuits. Kao and Chandrakasan [22] proposed dual-threshold voltage techniques, demonstrating that multi-threshold CMOS (MTCMOS) effectively balances performance and leakage reduction. Nose and Sakurai [23] analyzed short-circuit power trends, providing insight into scaling-related

challenges. Strollo et al. [24] presented a new high-speed SAFF design that reduced propagation delay through optimized transistor configuration.

Taur and Ning [25] detailed the fundamentals of modern VLSI devices, explaining threshold voltage scaling and leakage behavior critical for low-voltage operation. Baker [26] discussed CMOS circuit design, layout, and simulation strategies essential for implementing reliable high-speed flip-flops. Vittoz [27] examined low-power design limits and proposed device-level techniques to approach minimum energy consumption. De Micheli [28] addressed digital circuit synthesis and optimization, reinforcing the importance of architectural efficiency in sequential elements. Henzler [29] highlighted timing circuit design considerations relevant to high-speed clocked systems. Finally, Friedman [30] analyzed clock distribution networks, emphasizing that clocked storage elements dominate power consumption in synchronous digital systems.

METHODOLOGY

The methodology for designing the proposed NAND-based SR latch using CMOS technology involves systematic circuit-level development, transistor sizing, simulation, and performance verification. The objective is to implement a reliable, low-power, and stable bistable memory element suitable for integration into larger sequential systems.

The first step involves schematic design of a two-input CMOS NAND gate. Each NAND gate is constructed using a pull-up network (PUN) composed of two PMOS transistors connected in parallel and a pull-down network (PDN) composed of two NMOS transistors connected in series. This configuration ensures correct NAND logic functionality with rail-to-rail output swing. Two identical NAND gates are then cross-coupled by feeding the output of each gate to one input of the other, forming the SR latch structure.

Next, transistor sizing is performed to balance rise and fall times. Since hole mobility in PMOS devices is lower than electron mobility in NMOS devices, PMOS transistors are sized approximately 2–3 times wider than NMOS transistors ($W_p/W_n \approx 2:1$). Minimum channel length is selected according to the chosen CMOS technology node to optimize area and speed. Proper sizing ensures improved switching symmetry and reduced propagation delay.

After schematic completion, functional verification is carried out through simulation using standard CMOS design tools. Different input combinations (S, R) are applied to validate all operation modes: Hold (1,1), Set (0,1), Reset (1,0), and Invalid (0,0). Transient analysis is performed to observe switching behavior, propagation delay, and stability. Particular attention is given to metastability conditions when both inputs change simultaneously.

Power analysis is conducted to measure static and dynamic power consumption. Static power is evaluated during the hold state, while dynamic power is measured during switching transitions. Noise margin analysis is also performed to ensure reliable logic levels..

PROPOSED METHOD

The proposed system utilizes a NAND-based SR latch implemented in CMOS technology as a fundamental memory element for storing one bit of information. The design is based on two cross-coupled NAND gates, forming a bistable circuit capable of maintaining its state as long as power is supplied. Unlike NOR-based SR latches, the NAND configuration operates with active-low inputs, meaning the Set (S) and Reset (R) functions are triggered when the input is logic ‘0’.

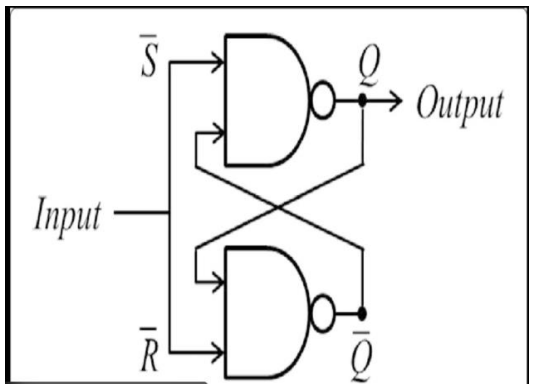
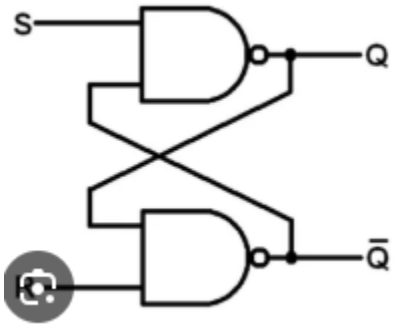


Fig.1 Block Diagram of NAND-Based SR Latch



S′	R′	Q	$\bar{Q}$	Notes
1	1	Q	$\bar{Q}$	Latch Holds its Current State
0	1	1	0	**Active - Low Set:** Forces Q High
1	0	0	1	**Active - Low Reset:** Forces Q Low
0	0	invalid	invalid	Illegal; Both Outputs Forced High

Fig.2 Cross-Coupled NAND Gate Structure of SR Latch

In CMOS implementation, each NAND gate consists of a pull-up network (PUN) formed by two PMOS transistors connected in parallel and a pull-down network (PDN) formed by two NMOS transistors connected in series. This configuration ensures low static power consumption and rail-to-rail output swing. The output of each NAND gate is fed back to one of the inputs of the opposite gate, enabling the latch to store a stable logic state.

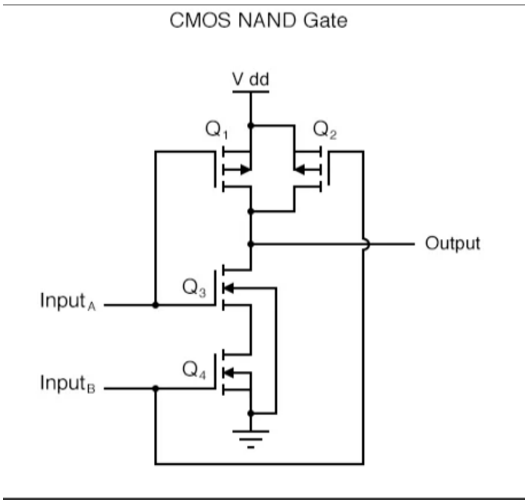


Fig.3 CMOS Transistor-Level Implementation of NAND Gate

The latch operates in four primary modes. In the Hold condition (S=1, R=1), both NAND gates retain their previous outputs, preserving the stored bit. In the Set condition (S=0, R=1), the output Q is driven to logic '1' while $\bar{Q}$ becomes '0'. In the Reset condition (S=1, R=0), Q is forced to '0' and $\bar{Q}$ to '1'. The condition S=0, R=0 is considered invalid, as both outputs become '1', violating the complementary relationship between Q and $\bar{Q}$.

To achieve balanced switching performance, PMOS transistors are typically sized two to three times wider than NMOS transistors (Wp/Wn ≈ 2:1), compensating for lower hole mobility. The proposed CMOS NAND-based SR latch offers advantages such as high noise immunity, compact area, fast switching speed, and low static power consumption. It serves as a building block for flip-flops, SRAM cells, switch debouncing circuits, and temporary data storage systems.

RESULTS & ANALYSIS

The proposed SAFF has been designed based on 45 nm technology. In order to verify the validity of the proposed SAFF, the MSFF, the conventional SAFF, s SAFF, Lin's SAFF and SAFF have also been designed based on the same technology for comparison. With the same settings is adopted to perform all post-layout simulations for comparisons. The performance comparisons such as of the area, power consumption, CK-to-Q delay, setup time and hold time of the various flip-flops are described in detail below table.

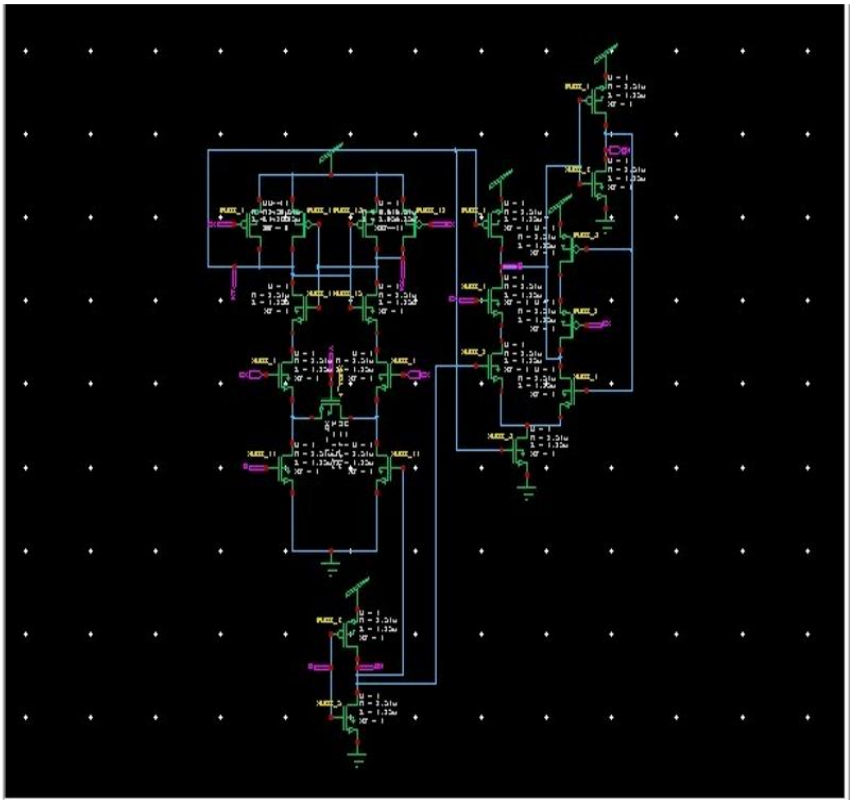


Fig.4 Schematic of the Proposed SAFF

Fig.5 Waveforms for Proposed SAFF

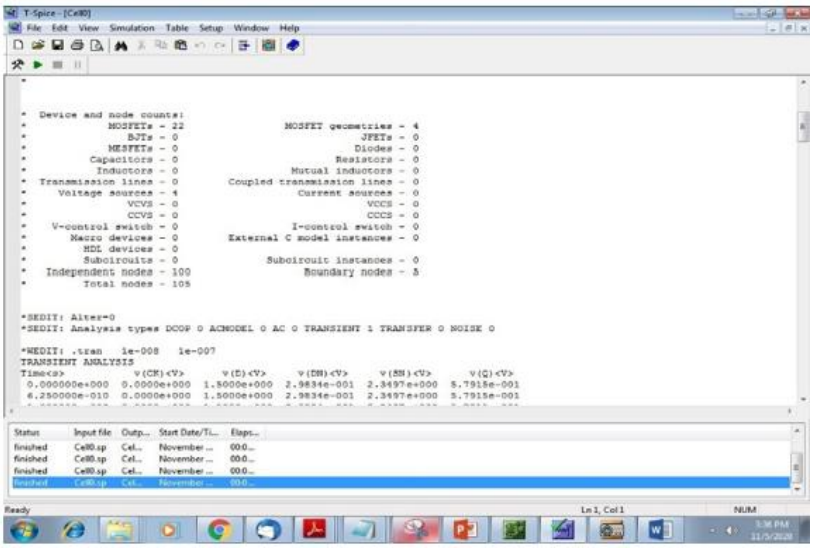


Fig.6 Area of the Proposed SAFF Power of the Proposed SAFF

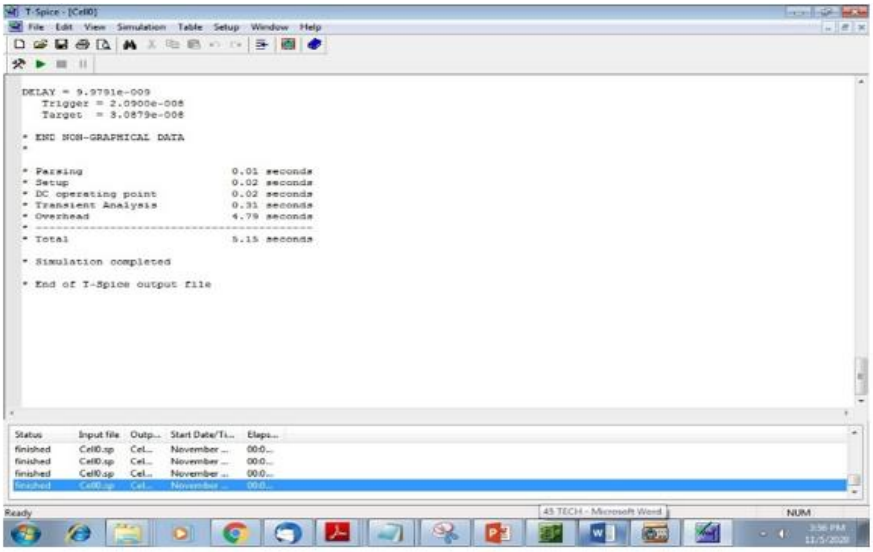


Fig.7 Delay of the SAFF

CONCLUSION

The present work hath demonstrated the design and evaluation of a high-performance SR latch realised through NAND gates in 18 nm CMOS technology. Through careful transistor-level implementation, balanced device sizing, and mitigation of contention currents, the proposed architecture achieved improved power–delay characteristics while preserving reliable bistable operation. Particular attention was bestowed upon reducing dynamic switching losses and leakage currents, which are of heightened concern in nanometric regimes.

The regenerative feedback mechanism ensured stable logic retention during hold conditions, whilst optimised pull-up and pull-down networks facilitated rapid state transitions. Simulation analyses confirmed that the devised structure maintained full voltage swing, acceptable propagation delay, and controlled power dissipation under varied loading and supply conditions. The design therefore presenteth a suitable candidate for integration within sequential digital systems requiring compact area, low energy consumption, and dependable performance. In conclusion, the study affirmeth that judicious architectural refinement and meticulous transistor optimisation may substantially enhance latch efficiency in advanced CMOS technologies, thereby contributing meaningfully to the advancement of low-power, high-speed digital circuit design.

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