International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463
Vol. 4 Issue 6, June-2015, pp: (210-218), Impact Factor: 1.252, Available online at: www.erpublications.com

Performance analysis of Low power CMOS Op-Amp

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Abstract: This paper proposes a low power CMOS operational amplifier which operates at 1.8 V power supply. The unique behavior of the MOS transistors in sub-threshold region not only allows a designer to work at low input bias current but also at low voltage. While operating the device at weak inversion results low power dissipation but dynamic range is degraded. Designing of two-stage Op-Amp is a multi-dimensional optimization problem where optimization of one or more parameters may easily result into degradation of others. The Op-Amp is designed to exhibit a unity gain frequency of 17.3 MHz and exhibits a gain of 62.04dB. The proposed design uses a smaller compensation capacitor (CC), which improves the slew rate and also, benefits for the area of compensation circuit. In order to verify the viability two-stage Op-Amp at SCNO 180 nm CMOS technology is designed and verified and power consumption is reduced.

Keywords: Low power CMOS Op-Amp, gain bandwidth product, gain margin, phase margin.

INTRODUCTION

Operational amplifiers (op amps) are the most versatile and an integral part in various analog and mixed-signal circuits. The term OTA was originally conceived for operational transconductance amplifiers with linear transconductance (used for the implementation of continuous-time filters), for the sake of simplicity we will use the same term OTA for general operational trans conductance amplifiers. The two-stage Op-Amp shown in Fig. 1 is widely used because of its simple structure and robustness. The method handles a very wide variety of specifications and constraints, is extremely fast, and results in globally optimal designs [1]. In designing an Op-Amp, numerous electrical characteristics, e.g., gain-bandwidth, phase margin common-mode range, offset, all have to be taken into consideration [2]. Furthermore, since Op-Amps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability [3]. Unfortunately, in order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised [4]. As a result, designing an Op-Amp that meets all specifications needs a good compensation strategy and design methodology. Designing high-performance analog integrated circuits is becoming increasingly exigent with the flexible trend toward reduced supply voltages [5]. Speed and accuracy are two most important properties of analog circuits, however optimising circuits for both aspects leads to contradictory demands. At large supply voltages, there is a tradeoff among various performance parameters. The realization of a CMOS Op-Amp that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem. The simulation results have been obtained and verified using 180nm SCNO MOSIS Design and carried out in Cadence virtuoso.

PERFORMANCE PARAMETERS

Following are various operational amplifier performance parameters.

Large signal voltage amplification

The open loop gain of an op amp determines the precision of the feedback system employing the op amp. The required gain can be adjusted according to the application. Trading with the parameters such as speed and output voltage swings, the minimum required gain must therefore be known. A high open loop gain is also necessary to suppress nonlinearity. Av is the ratio of the peak-to-peak output voltage swing to the change in input voltage.

$$A_V = V_O / V_{IN} \qquad (1)$$

Unity Gain Bandwidth (UGB)

The product of the open-loop voltage amplification and the frequency at which it is measured is called UGB.

$$GBW=A_v * \text{Frequency} \quad (2)$$

Common-Mode Rejection Ratio (CMRR)

The ratio of differential voltage amplification to common-mode voltage gain is called CMRR. CMRR falls off as the frequency increases.

$$CMMR = A_{DIFF} / A_{COM} \quad (3)$$

This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.

Slew Rate

The average time rate of change of the closed-loop amplifier output voltage for a step-signal input

$$SR = dv/dt \quad (4)$$

In op amps we trade power consumption for noise and speed. To increase slew rate, the bias currents within the op amp are increased.

Gain Margin

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input

Phase Margin

The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity. Gain and phase margins are measures of stability for a feedback system, though often times only phase margin is used rather than both.

TWO STAGE CMOS OP-AMP

The two stage op-amp will be used to introduce the concept of compensation show in fig-1. The goal of compensation is to maintain stability when negative feedback is applied around the op-amp The basic equations and parameters are described below. These design main parameters are: phase margin (MΦ), gain-bandwidth product (GBW), load capacitance (CL), slew rate (SR), input common mode range (ICMR),In this circuit replacing the current source and uses PMOS active load.

Drain current of cmos is given as

$$I= \mu 0 Cox \frac{W}{L} \frac{(Vgs-Vt)^2}{2} \quad (3.6)$$

We know that

$$\frac{1}{r} = Gm = KS\,(Vgs - Vt) \quad (5)$$

Using formula in current and resister and accepted ratio

$$r = 1/K'S\,(Vgs-Vt) \quad (6)$$

Where S=W/L

K'=μ0Cox

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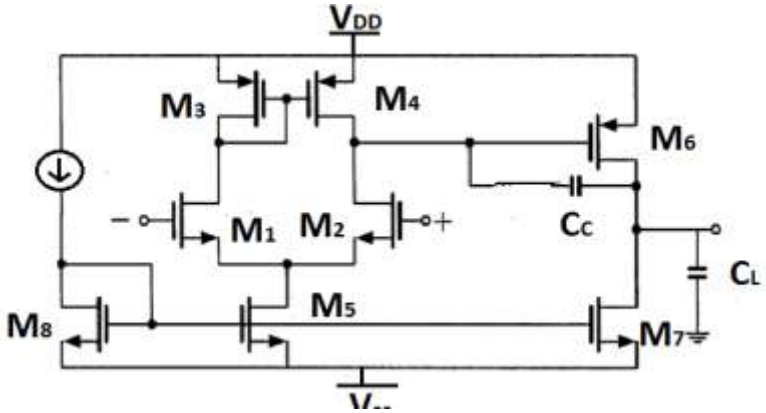

Figure 1: Two stage op-amp

For two-stage CMOS op amp, the simplest compensation technique is to connect a capacitor across the high gain stage. This results in the pole splitting phenomena which improves the closed-loop stability significantly. However, due to the feed-forward path through the Miller capacitor, a right half-plane (RHP) zero is also created. An uncompensated right half-plane zero drastically reduces the maximum achievable gain-bandwidth product, since it makes a negative phase contribution to the open-loop gain at a relatively high frequency. In order to compensate the right-half plane zero, an appropriate design approach is essential. Such a zero can be nullified if the compensation capacitor is connected in conjunction with either a nullifying resistor or a common-gate current buffer. After compensation of right half-plane zero, the maximum gain-bandwidth product is limited by second pole.

DESIGN PRODUCER OF TWO STAGE OP-AMP

For simplicity, both the mobility reduction due to the normal field and the velocity saturation effect associated with MOS devices will be neglected. The following MOSFET, strong-inversion, square-law equations:

$$I_D = \frac{\mu_{n,p} C_{ox}}{2}\left(\frac{W}{L}\right) V_{eff}^2 \qquad (7)$$

$$g_m = \sqrt[2]{2\mu_{n,p} C_{ox} \frac{W}{L} I_D} \qquad (8)$$

$$g_m = \frac{2I_D}{V_{eff}} \qquad (9)$$

Where $V_{eff} = V_{GS} - V_{tn}$ for NMOS $V_{eff} = V_{GS} - V_{tp}$ for PMOS, is used throughout the design. Strong inversion typically requires values of V_{eff} greater than approximately 200 to 250 mV for bulk MOSFET's at room temperature. The small signal transfer function of the CMOS according to the equivalent circuit shown in Figure 3.3 is

$$A(s) = \frac{\omega_u}{s} \times \frac{1 - sC_C\left(\frac{1}{g_{m6}} - R_C\right)}{1 + \frac{C_{gs6}C_L + C_{gs6}C_C + C_C C_L}{g_{m6}C_C} s + \frac{R_C C_{gs6} C_L}{g_{m6}} s^2} \qquad (10)$$

Where

$$\omega_u = A_0 \omega_{p1} = \frac{g_{m1}}{C_C} \qquad (11)$$

is the unity-gain frequency, also commonly known as gain- bandwidth product, of the op-amp. The dc gain of op-amp is given by

$$A_0 = g_{m1}g_{m6}R_AR_B \quad (12)$$

and op-amp's dominant pole frequency can be given as

$$\omega_{p1} = \frac{1}{g_{m6}R_AR_BC_C} \quad (13)$$

BASIC OPERATIONAL AMPLIFIER EQUATIONS

Output Swing

Defining V_{HR}^{out} as the op amp head room voltage at output, according to Figure3.1

$$V_{HR}^{out+} = V_{DD} - V_{out(max)} \quad (14)$$

$$V_{HR}^{out-} = V_{out(min)} - V_{ss} \quad (15)$$

Which yield,

$$V_{HR}^{out+} = V_{eff6} \quad (16)$$

$$V_{HR}^{out-} = V_{eff7} \quad (17)$$

Common-Mode Range (CMR)

If V_{HR}^{CM} is definesd as the op-amp head room voltage of the input common-mode range i.e.,

$$V_{HR}^{CM+} = V_{DD} - V_{CM(max)} \quad (18)$$

and

$$V_{HR}^{CM-} = V_{CM(min)} - V_{SS} \quad (19)$$

according to Figure3.1,it can be shown that

$$V_{HR}^{CM+} = V_{eff3} - V_{tn} \quad (20)$$

$$V_{HR}^{CM-} = V_{eff5} + V_{tn} + V_{eff1,2} \quad (21)$$

Internal Slew Rate

The slew rate associated with C_C can be found to be

$$SR = \frac{I_{D5}}{C_C} \quad (22)$$

External Slew Rate

The slew rate associated with C_L can be found to be

$$SR = \frac{I_{D7}-I_{D5}}{C_L} \quad (23)$$

Combining (22) and (23)

$$I_{D7} = SR(C_C + C_L) \quad (24)$$

Offset Voltage

Systematic offset is caused by current imbalance in the output stage i.e., between I_{D6} and I_{D7} , when there is no input voltage. Under such condition,

$$I_{D3} = I_{D4} = \frac{I_{D5}}{2} \qquad (25)$$

SIMULATION RESULT

Simulation result of op-amp using mosis fabrication library and electrical specification of CMOS op-amp show in table 1 in load capectiance 10 pf and supply voltage 1.8 volt .table 2 show process parameters**.**

Table 1: ELECTRICAL SPECIFICATION OF CMOS Op-amp

Load capacitance: C_L (pF)	10
Miller compensation capacitances: C_C (pF)	3
Supply voltage	+1.8 V

Table 2: PROCESS PARAMETERS (SCNO180 nm Tech.)

$\mu C_{ox}/2$: NMOS (A/V^2)	173.9
$\mu C_{ox}/2$: PMOS (A/V^2)	35.0
$V_{th,p(min)}$ (volt)	0.37
V_{thnmax}(volt) NMOS	0.50
ICMR(Volt)	1.3
Vdd(volt)	1.8

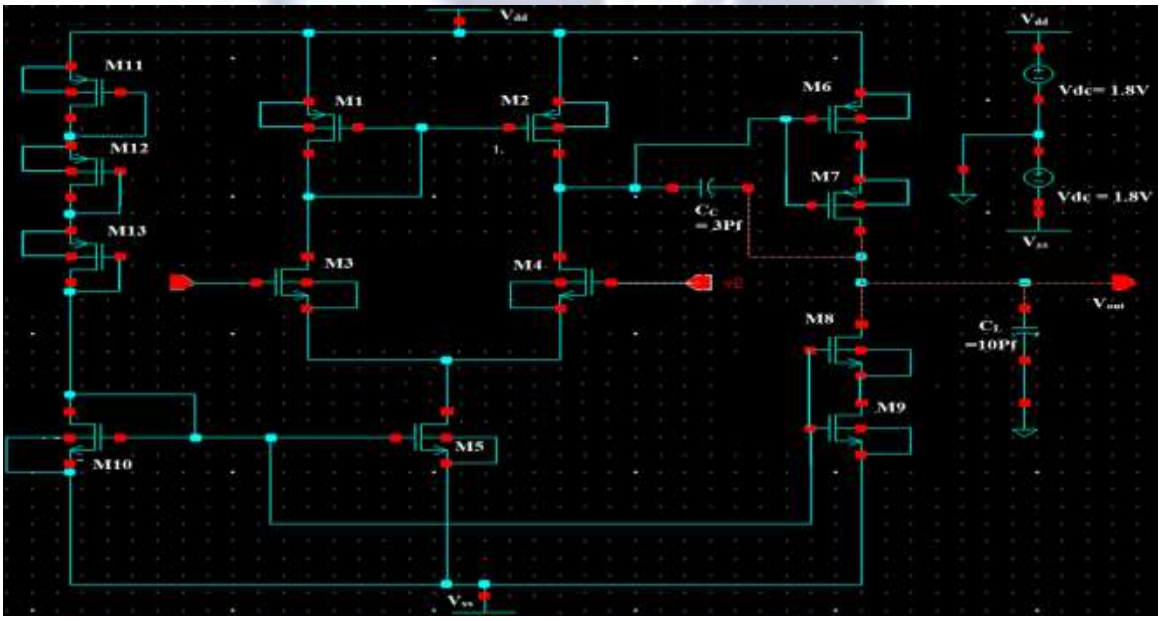

Figure 2: Two stage Op-amp

AC Response

Through AC response we can simulate the schematic to find out the bode plot and phase plot. In Figure 3, a bode plot and phase plot for 1.8 V, 27° C and C_L = 10 pf is shown. As it can be seen, the open loop gain is 62.05 dB, and a phase margin is 166.3°. The unity gain bandwidth is 17.15MHz bandwidth is 1.74 KHz.

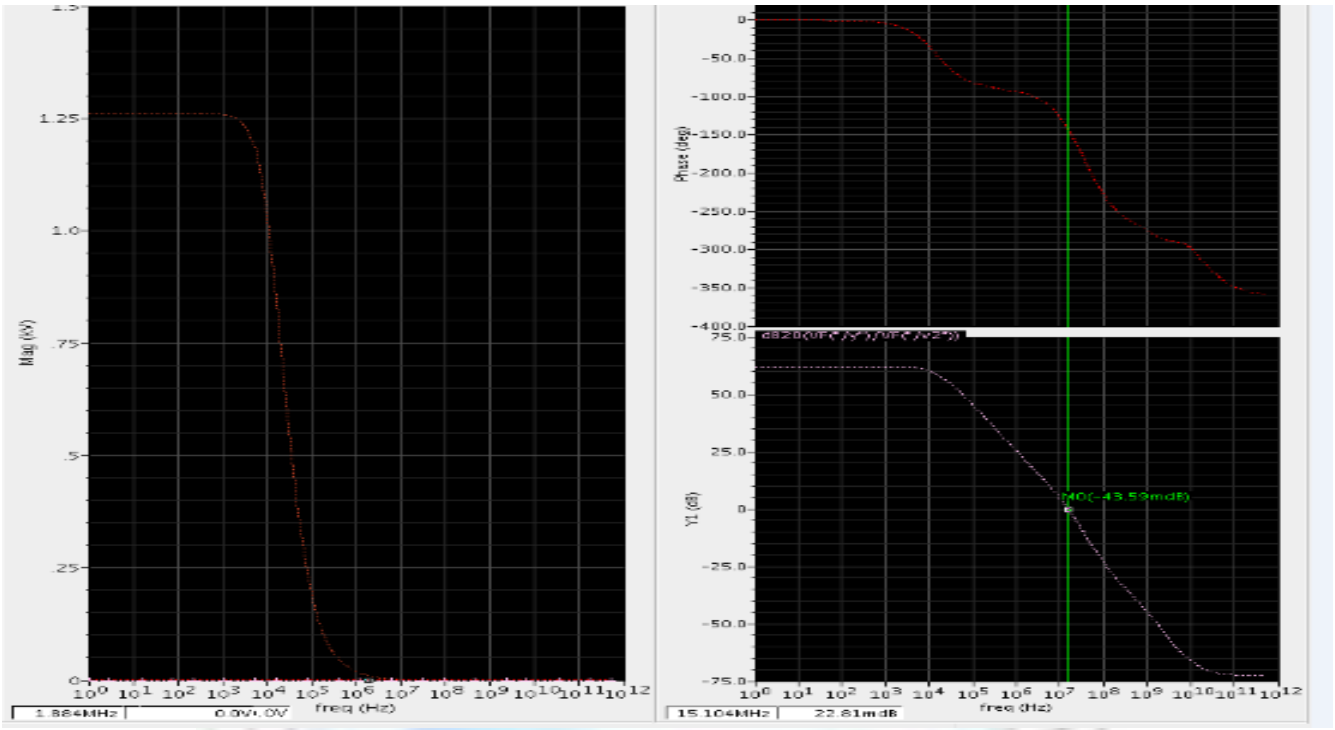

Figure-3: Characteristics of AC Response

Transient Step Response

In Figure 4, a step from ground to VDD is applied at the input with unity feedback configuration. The slew rate of op-amp is 11.23 V/µS for rising edge of pulse and 11.10 V/ µS for falling edge of the pulse.

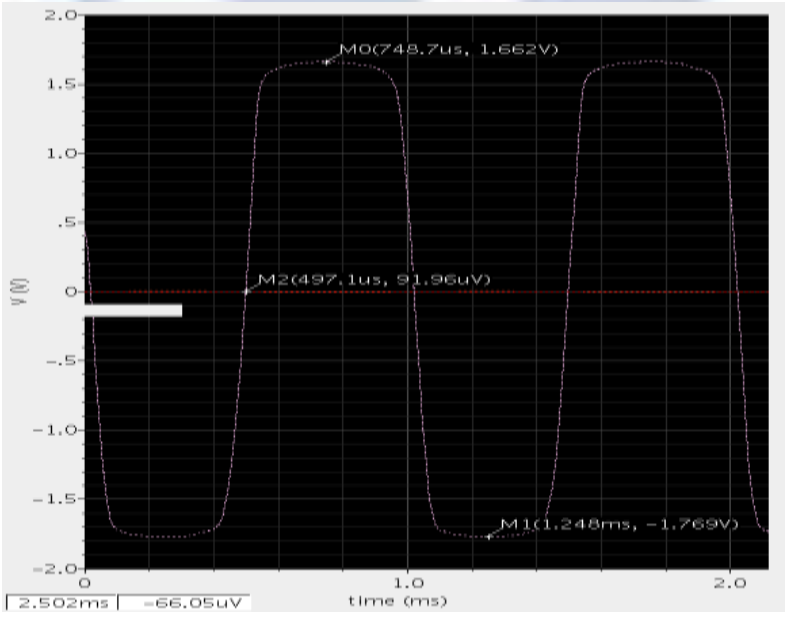

Figure 4: Characteristics of Transient step Response

Gain and Phase:

The open-loop gain of an operational amplifier falls very rapidly with increasing frequency. Along with slew rate, this is one of the reasons why operational amplifiers have limited bandwidth-Fig-5 shows DC gain and phase. Its represent DC gain is 62db and phase 179 deg.

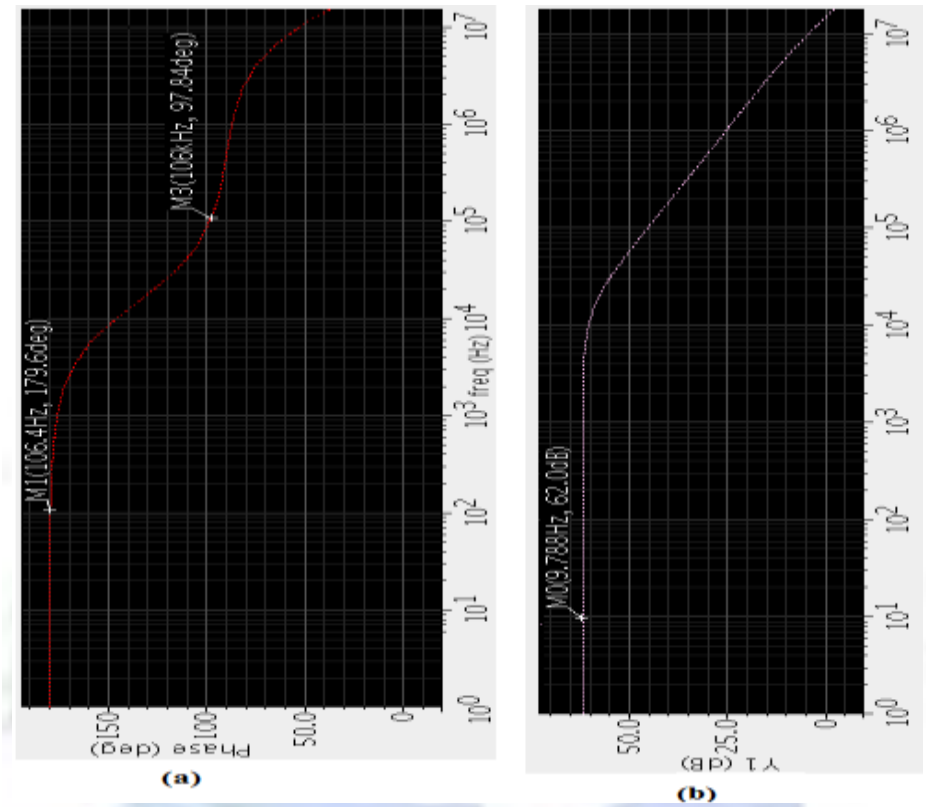

Figure 5 - Characteristics of Phase and Gain

Gain Margin, GM, Phase Margin, PM:

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity. Gain and phase margins are measures of stability for a feedback system, though often times only phase margin is used rather than both. Based the magnitude response of the loop gain. Fig:6 show phase margin and gain margin.

Gain margin is a measure of closeness of phase crossover point to (−1, j0). in GH plane. At phase crossover ωc, GH = G(jωc)H(jωc).

$$\text{Gain margin} = 20\log 10|G(j\omega c)H(j\omega c)|$$

is Usually positive. If gain is increased and |GH| goes through (−1, j0), the system has gone unstable. If GH never cuts negative axis the system is forever stable. Gain margin is the amount of gain in dB that can be allowed to increase in the loop before closed loop system reaches instability. Phase Margin is how much to rotate the gain crossover point so that you go through (−1, j0).

Phase margin is defined as the angle in degrees through which the G(ω)H(ω) plot must be rotated about the origin in order that gain crossover point on locus passes through (−1, j0) point. φM = 6 GH – 1800

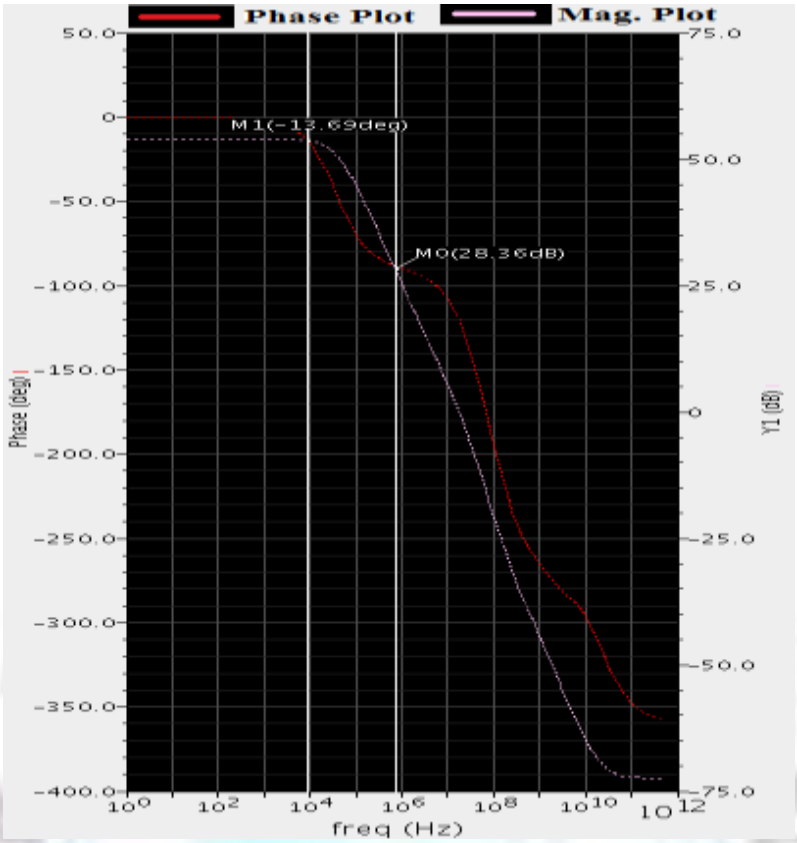

Figure 6: Characteristics of Gain margin and Phase margin

Table 3 : Simulation Results of Op-Amp (180nm Technology)

Simulation result of two stage op-amp show in table -3

Specifications	**Theoretical value**	**Simulation results**
DC gain (dB)	**54**	62.05
GB (MHz)	17.3	18.9
Phase margin		166.31
CMRR (dB)	**159.5**	-
ICMR (V)	1.3	1.0
Slew rate (V/µS)	10.8	11.23
Power dissipation(µW)	121.4	-
I_{D5}(µA)	32.4	33.78
I_L(µA)	140.4	141.8
Load capacitance (pf)	10	10
Supply voltage (V)	1.8	1.8
Gain margin		28.36

CONCLUSION

We have realized two stages Op-Amp in 180 nm CMOS technology. By the proposed structure we got excellent result of dc gain and Slew rate. If it is less than the simulated one (not totally realistic, because technology dispersion are not taken into account) dc gain and GBW shows increase DC gain decrease GBW frequency .then I say that yet increase bandwidth of op-amp then balance DC Gain , good being to amplifier. if increase frequency then these amplifier work at oscillator .so we have to balance condition in both. We do not have yet the simulation result for the Op-Amp realized at 180 nm with 1.8 V V_{DD}.

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