Carbon Nanotube Fet Based Full Adder

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Abstract: High speed Full-Adder (FA) module is an important element in designing high performance arithmetic circuits. In this paper, I propose a high speed multiple-valued logic FA module. The proposed FA is designed and constructed with the use of 3 capacitors and 14 transistors, where the transistors are constructed by carbon nano-tube field effect transistor (CNFET) technology. Furthermore, my proposed technique has been examined in different voltages (i.e., 0.65v and 0.9v). The observed results reveal power consumption and power delay product (PDP) improvements compared to existing FA counterparts.

Keywords: Carbon Nanotube; Carbon Nanotube Field Effect Transistor; Full Adder; High Speed; Mulitple Valued Logic.

Introduction

Over the past years, silicon-based electronic technology has been improved through the use of MOSFETs, which has resulted in higher device performance. However, there are still some obstacles related to scaling.One such could be that the diffusion areas will no longer be separated by a low doped channel region and equivalent gate oxide thickness will fall below the tunnelling limit. Hence, there is a need to extend or complement traditional silicon technology. As one of the promising technologies which is considered most promising, nanotechnology avoids most of the fundamental limitations for conventional silicon devices. Nanotechnology when used in electronics circuit design is termed as nanoelectronic is an applicable that is producing nanoscale machine components and systems efficiently, such as nanowires, nanoparticles and Carbon Nano Tubes (CNT). CNTs have special properties(electronic, mechanical and thermal) that make them promising for the future use in field of integrated circuits. Transistors which have carbon nanotubes as their channel are called Carbon Nanotube Field Effect Transistor (CNFET). Recently, some circuit applications are presented based on CNFETs, such as ring oscillators, invertors, and logic gates [1], [2]. Arithmetic operations are extensively used in many VLSI applications such as signal processing, and digital communications [3], [4]. Adders are major part of computational circuits that are used for implementing any other arithmetic operation such as subtraction, multiplication or even logarithmic functions[1],[5]. Hence, it is important to construct very efficient addres as they affect the performance of the system. Many logic combinations have been tried and implemented to produce efficient full adder circuit. The complementary CMOS and CPL designs are two conventional Adders based on CMOS structure. Based on transmission function and transmission gate, TFA and TGA designs were implemented. The other designs are classified as Hybrid designs. Applying DOI : 10.5121/vlsic.2011.2101 [1]. CNFETs in Full Adder cells will lower the propagation delay and lower the power consumption of circuit.

Carbon Nanotube Field Effect Transistors (CNFET)

Carbon Nano Tubes (CNTs) consist of sheets of graphene rolled into a tube [5]. Depending on their chirality (i.e., the direction in which the graphite sheet is rolled), the single-walled carbon nanotubes can either be metallic or semiconducting[1]. CNFETs are the molecular devices that don't follow the most fundamental silicon transistor restriction and have very high speed transport in their channel [6], [7]. Hence a CNT is most suitable for their use in field effect transistor(FET).

By using appropriate diameter suitable threshold voltage for CNFET can be achieved. The threshold voltage of the CNFET is proportional to the inverse of the diameter of CNT and can be expressed as [1]:

$$V_{th} = \frac{0.42}{d(nm)} \qquad (1)$$

For a CNT which has (a, b) as chirality the equation for C--C distance is given by [8]:

$$D_{CNT} = \frac{0.078\sqrt{a^2+b^2+ab}}{1} \qquad (2)$$

There are two kinds of CNFETs based on the connections between the source and the drain. At the source channel junction tunneling takes place through Schottky barrier [9]; hence, these transistors are called Schottky Barrier CNFET (SB-CNFET).

SB-CNFET have ION/IOFF ratio because Schottky Barrier doesnot allow trans conductance.[10]. Second device is MOSFET-like CNFET which is doped in un-gated portions and has similar behaviour to CMOS transistors and it presents unipolar behaviour [11].There is no schottky barrier hence higher ION unlike SB-CNFETs. CNFETs have high on-off ratio compared to schottky barrier transistors[7].

Multiple Valued Logic

In Multiple Valued Logic there may be more than one truth values. MVL circuits can be used to implement various functions with reduced number of components and hence they improve the overall performance of the circuit[12].

Previous Works

Improvements have been made in the design of the components so as to have low power consumption, reduced chip size, high speed, and maximum throughput.Full Adder is a vital part of a processor's ALU(Arithmetic Logical Unit)[14-16]. There are two ways of designing a Full Adder cell. In classical designs only single logic style is used for the whole cell, whereas hybrid FA use more than one logic style in a cell [13]. Other logic is complementary pass transistor logic (CPL). In CPL SUM and CARRY are implemented separately. CPL is a high speed logic style but with high propagation delay due to presence of large number of internal connections [14]. CPL uses 32 transistors which increases the complexity of the circuit. Hybrid CMOS FA comprises of three modules: First module generates intermediate signals which are passed to second and third modules and it can be XOR-XOR, XOR-XNOR, XNOR-XNOR [17],[15],[16]. Second produces SUM and third produces CARRY example, Static Energy Recovery Full Adder (SERF) that uses 10 transistors. Majority function logic circuit can be used to find the C_{out} of the circuit with odd (here three) number of inputs. The majority function is represented as (3):

$$\text{Majority } (A,B,C)= AB+AC+BC= C_{out} \tag{3}$$

Majority-not gate can be created with the help of capacitors and CMOS. In CMOS Technology complementary gates(NAND, NOR etc.) can be implemented by scaled Inverters [17]. Different design of majority-not based Full Adders have been shown in [1][25-28]. These circuits are implemented in two stages as shown in Fig 1. Carry Out has similar function, but in SUM output differ in circuit structure and the transistor count. The first stage is producing $\overline{C_{out}}$ by means of majority-not function and in the second stage SUM is generated by means of functions F that implemented in different styles. These Full Adders consume less power than known designs as less transistors are used in our design.[17]

Full Adder having first majority not has the function of kind:

$$\text{SUM} = \text{Maj}(A,B,C,C_{out})[17] \tag{4}$$

In our design two stages majority-not function is used first one for C_{out} and next stage as five input majority-not function for creating Sum. The logic of [17] is made of two parallel connected NMOS and PMOS transistors that provide a path to the input. Transistor count is 8 and capacitor count is 7.
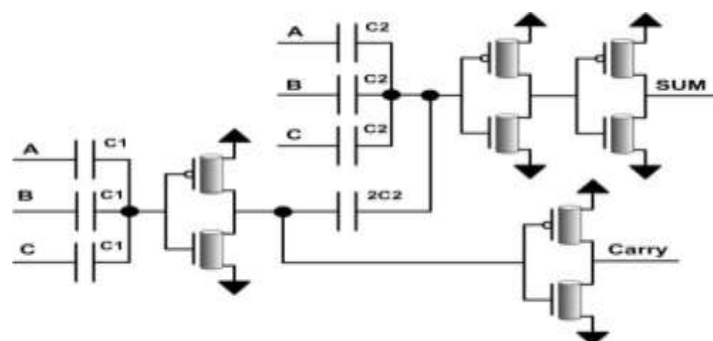

Figure. 1. Full Adder Design CNT-FA1 [17]

The another design low-voltage CNFET-based Full Adder circuit based on Minority Function presented in [18] uses only 8 transistors and reduces the number of capacitors to 5 as shown in fig 2, but uses capacitors in the middle of design which result in reduction in speed. The $\overline{\text{Cout}}$ implemented by majority-not function too.

In next design [19], NAND and NOR gates are used for implementing Sum as equation of

$$SUM = Maj(A,B,2*NANAD(A,B,C),2*NOR(A,B,C)).$$

Overall performance is improved as the number of capacitors used are less. Figure 3.
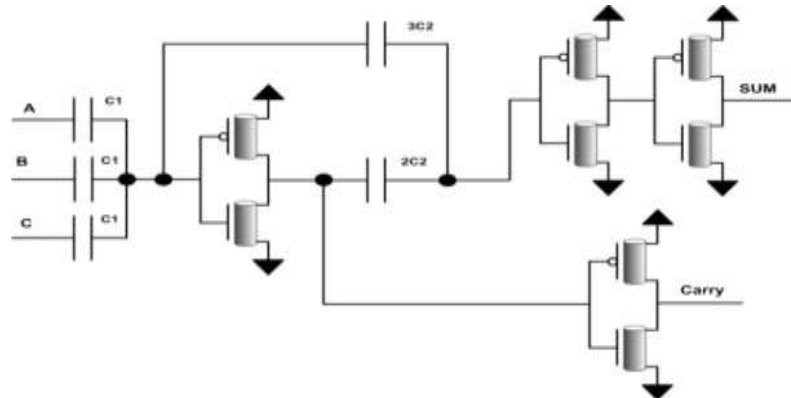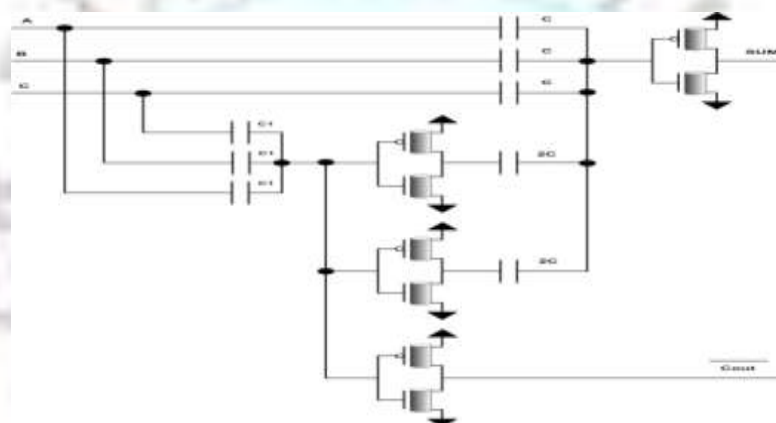

Figure.2. Full Adder Design CNT-FA3 [18]

Figure 3. Full Adder Design CNT-FA2 [19]

Proposed Full Adder

One method to implement majority-not function is using basic inverter and three capacitors connected to the inputs of inverter as presented in Fig 4. In design of majority-not function, three capacitors are implementing Multiple-Valued logic levels.

$$\text{The levels are } 0, \frac{V_{DD}}{3}, \frac{2V_{DD}}{3}, V_{DD}$$

The inverter threshold voltage is regulated so that it will be OFF when most number of inputs are '1'. The circuit can be used as Either NOR or NAND functions if inverter transistors have different threshold voltage in Fig.4.
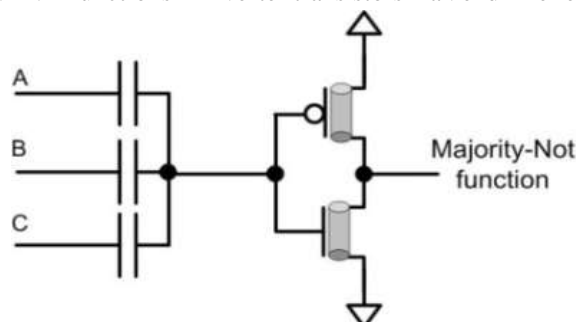

Figure 4. Majority-not Function Circuit

For NAND function, when three inputs (A, B, C) are all '1', output should be '0' otherwise output should be '1'. For NOR function if there is one input that is '1', output should be '0' otherwise output should be '1'. As in sum formula (4) output can implemented by NOR, NAND and majority-not functions and Fig. 5 and formula (5) will be attained.
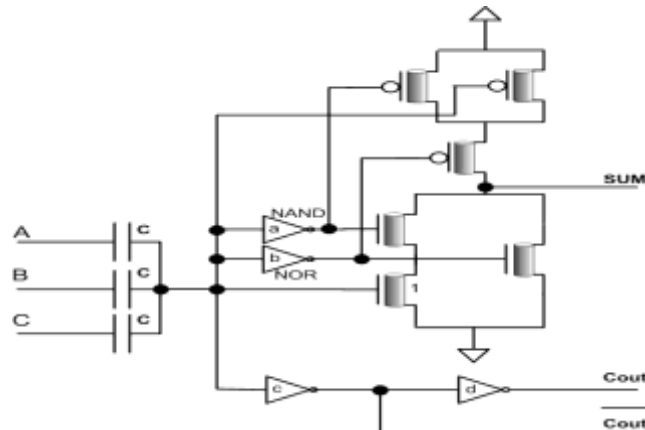

Figure.5. Proposed Full Adder design(5)

In proposed Adder I use less capacitors rather than contemporary CNFET Adders. The simulation results indicate that this reduction has caused our Full Adder cell to become much faster. This design presents a circuit which uses 14 transistors and 3 capacitors and also produces carry and outputs. Outputs of the circuit will be connected to power supply or ground. When at least one input is '1', the transistor marked with '1' will act as a majority function and becomes ON. The proposed design is full swing and in comparison to previous designs uses fewer capacitors.

Simulation Results

The Synopsys HSPICE circuit simulator has been used to simulate Full Adder circuits. The simulation results have been referenced from [1]. The circuits of C-CMOS, CPL, TGA and Hybrid are simulated using 32nm MOSFET technology. For simulating CNFET-based circuits the proposed compact model in [7] is used. Circuits are compared on the basis of propagation delay, power consumption and power delay product (PDP). For being more realistic, buffers (two cascaded inverter) are placed at the outputs. Our design is compared with known MOSFET designs and earlier CNFET Full Adder designs CNT-FA1 [17] CNT-FA2 [19] and CNT-FA3 [18]. Table 1 and 2 shows the value of power, delay and PDP for Hybrid, CMOS, TGA, CPL, CNT-FA1, CNT- FA2 and CNT-FA3. Various designs of CNFETs are simulated in 0.9v and 0.65v. Delay is studied from middle of the input voltage swing to the middle of the output voltage swing.[1] Simulation results in Table 1 and 2, indicate that the smallest delay belongs to the proposed Full Adder cell[1]. PDP is calculated as a trade-off between power consumption and delay. It is a measure of total performance of a circuit. Results show that that the proposed Full Adder has the best PDP.

Table I. Simulation Results for 0.9v

Design	Performance Parameters		
	Powerr	Delay	PDP
C-	6.26E-07	5.27E-11	3.30E-17
CPL	4.87E-07	1.57E-10	7.63E-17
TFA	6.32E-07	2.89E-10	1.83E-16
TGA	6.68E-07	3.46E-10	2.31E-16
Hybrid	4.96E-07	2.93E-10	1.45E-16
CNT-	1.05E-06	7.83E-11	8.20E-17
CNT-	3.32E-07	1.14E-10	3.80E-17
CNT-	7.83E-07	5.36E-11	4.20E-17
Proposed	**8.40E-07**	**1.25E-11**	**6.17E-18**

Table II. Simulation Results for 0.65v

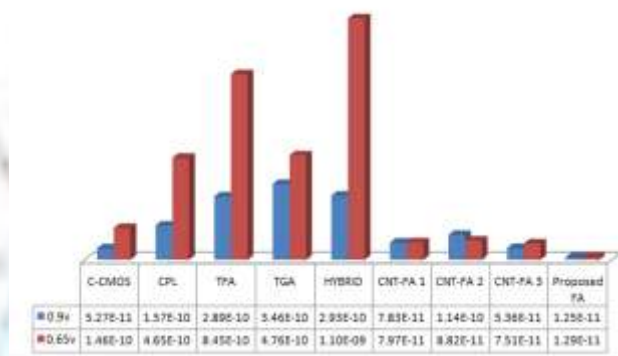| Design	Performance Parameters		
	Power	Delay	PDP
C-CMOS	2.94E-07	1.46E-10	4.28E-17
CPL	2.08E-07	4.65E-10	9.67E-17
TFA	1.52E-07	8.45E-10	1.29E-16
TGA	1.21E-07	4.76E-10	5.77E-17
Hybrid	1.71E-07	1.10E-09	1.88E-16
CNT-FA1	5.23E-07	7.97E-11	4.17E-17
CNT-FA2	4.71E-07	8.82E-11	4.15E-17
CNT-FA3	7.12E-07	7.51E-11	5.35E-17
Proposed Adder	**4.80E-07**	**1.29E-11**	**1.05E-17**

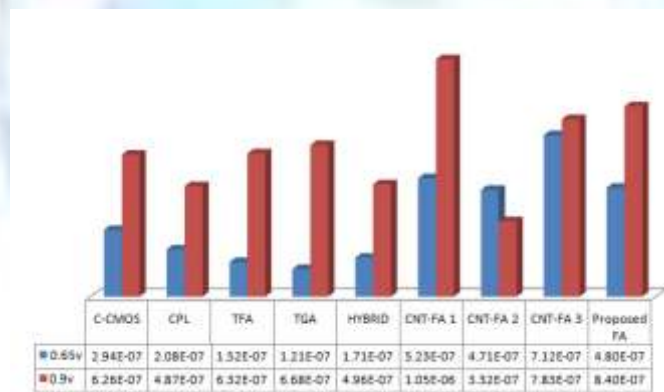**Figure 6. Propagation Delay comparison chart**

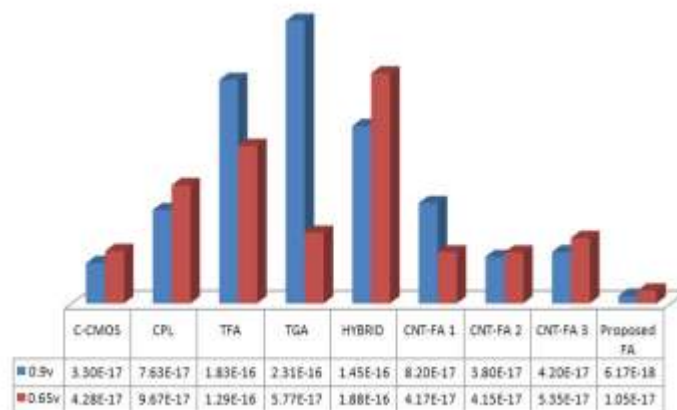**Figure 7. Power consumption comparison chart**

Figure 8. PDP comparison chart

Conclusion

In this paper a novel high speed majority based CNFET Full Adder has been proposed. Using CNFETs as a novel Full-Adder architecture improved the efficiency. The main concept of this design is implementing (5) using majority-not function and using majority-not circuit design as NOR and NAND functions by changing threshold voltage of CNFETs to produce intermediate signals. In order to evaluate the performance of the design, delay, power and power-delay- product (PDP) factors are compared with some of the state-of-the-art MOS and CNFET-based designs. Simulations have been performed on HSPICE by using CNFET technology in two voltages (0.9v and 0.65v). Eight other designs, including TFA, Hybrid, CMOS, TGA, CPL and previous three majority not based Full Adder designs are applied. Simulation results illustrate improvements in terms of delay and PDP in comparison to previous MOSFET and CNFET designs. There has been improvement in terms of power delay product(PDP) if we used our proposed Full-Adder cell as compared the best standard design amounts to 18% in 0.9v and 36% in 0.65v.

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