Design and Implementation of High Speed, High Data Rate Automatic Flywheel Logic for IRS Satellite Series

Srinivas R[1], Prof. Nithyananadan L[2], Subba Rao PVV[3], Umadevi G[4]

[1,3,4]Indian Space Research Organization, National Remote Sensing Centre, Balanagar, Hyderabad
[2]Electronics & Communication Engineering, Pondicherry Engineering College, Puducherry, India

Abstract: The Frame synchronizer code for IRS satellites is a PN sequence of 127bits. In the satellite data format the frame sync code has to be detected reliably and efficiently. During real-time when the serial data from satellite is being frame synchronized at ground station, there is a need of perfect frame synchronization at the ground otherwise the whole reference is lost. The frame synchronization once detected will be the frame sync which will be the master reference for decommutation of serial data. There can be a possibility and probability that in the video data bits there may be bits which can be similar to Frame sync code of 127bits. Hence in order to increase the reliability of frame sync detection and avoid the occurrence of false frame sync code detection flywheel logic is required.

Keywords: Frame sync; PN Sequence; IRS.

Introduction

The data from satellite is transmitted in S and X bands for IRS Series of satellites. The S band data is used for satellite data acquisition and SPS data to be received at ground station in S band chain. The video data for all IRS Series of satellites is transmitted in X band[2]. The Remote Sensing Satellite system can be divided into space segment and ground segment. Onboard the satellite there are different sensors one such is a active sensor and other one is passive. In case of the passive sensor, the reflected optical energy from the surface of earth with different reflection co-efficient is received by the CCD i.e. Charge couple device. The optical energy is converted into analogue signal; this is digitized with help of A/D converter. ,conversion to NRZL data and further processes like randomization and data formatting is done onboard the satellite[7]. In the process of data formatting the digital video data is formed into frame length packets of different lengths depending upon the satellite data rates. Here the frame length formats vary from 64K to 128K depending upon satellite and its data rate. So, whatever process is carried out onboard the satellite, exactly opposite process has to be done at ground station.

The data at ground station is to be retrieved faithfully without any kind of losses, data breaks; pixel drop outs etc. This is possible only when frame synchronization is done perfectly and efficiently. The flywheel design helps precise detection of frame sync code of 127 bits PN sequence and hence regulates the faithful retrieval of video data in real time[1]. Since, for IRS Satellites the data rates are varying from 42.4515Mbps to 320Mbps. It is necessary to design the flywheel logic to cater for low data rates to high data rates without any flaws. For example, taking into consideration, a basic data format length of 2400 bytes which is frame length of one of the IRS satellites[5], here in the typical frame length the frame sync pattern is followed by housekeeping data, auxiliary data and video data as shown in the figure-1.
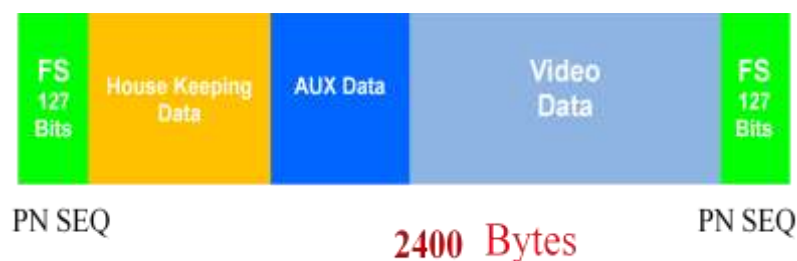

Figure 1 Typical Satellite data format

When the frame sync is detected, immediately the HK data, aux data and video data are stripped with reference of frame sync code[3]. Hence, if there is slight mismatch in detection of frame sync code then the entire video data reference is lost. Hence, flywheel basic purpose is to detect the frame sync reliably and efficiently. Since, the data format frame length is known the frame sync detection is enabled prior to the frame sync code and disabled in the video data portion[5]. This will enhance the reliability of frame sync detection logic. The basic concept of flywheel logic functioning is shown in figure-2.
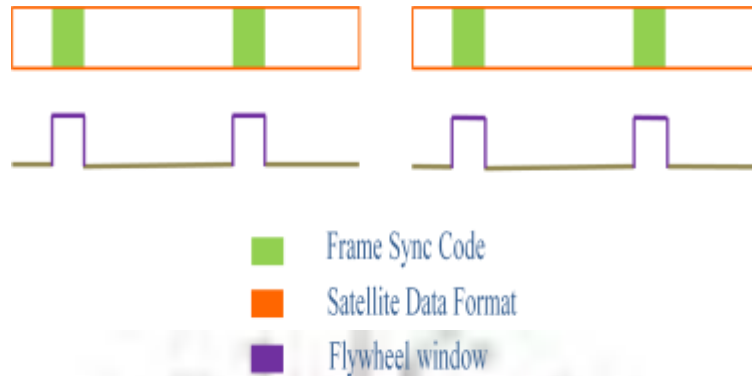

Figure 2: Flywheel basic concept

As shown in figure-2, the flywheel logic window is enabled only during frame sync code and disabled in the video data portion. Hence, there is no possibility of false frame sync detection, which will improve the performance and reliability of the frame sync logic circuit. The basic block diagram of flywheel design logic shown figure 3.
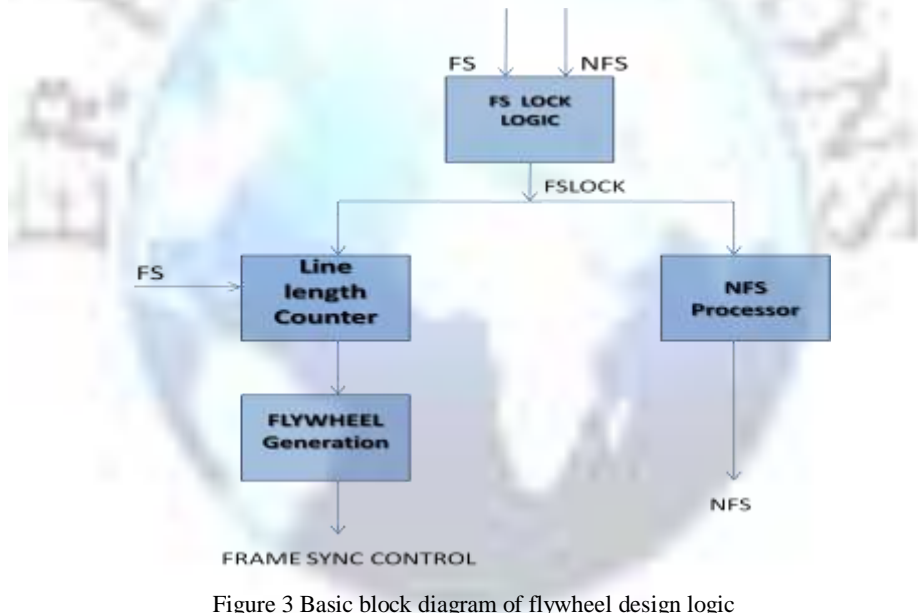

Figure 3 Basic block diagram of flywheel design logic

The frame sync pulse and NO frame sync pulse are given to the FS/ NFS lock logic when consecutive three continuous FS occurs it will generate FS lock. The FS lock output is given to line length counter and flywheel window generator. The FS pulse is also given to frame length counter depending upon the satellite frame length. The output of the line length counter is fed to NFS pulse generation. When consecutive three NFS are generated NFS processor will unlock the frame sync lock logic. Hence, the circuit goes into search mode. The Frame length counter and flywheel logic generates frame sync control signal.

Flywheel Design and Implementation

Flywheel logic takes the input signal i.e. frame sync pulse and NO frame sync pulse(NFS). Frame sync pulse is given to successive three FS sync pulse counter and NFS pulse is given to the same counter. As example, if after two successive frame sync pulse occurrence, next frame sync pulse is absent, NFS pulse will be generated in the period of FS pulse occurrence. This NFS pulse will reset the count two of successive three FS pulse counter. Thus only when three successive frame sync pulses occur this counter generates the output and it will set the lock flip flop and FS lock the signal. Like the above same mechanism for successive three NFS pulses FS lock will be reset.
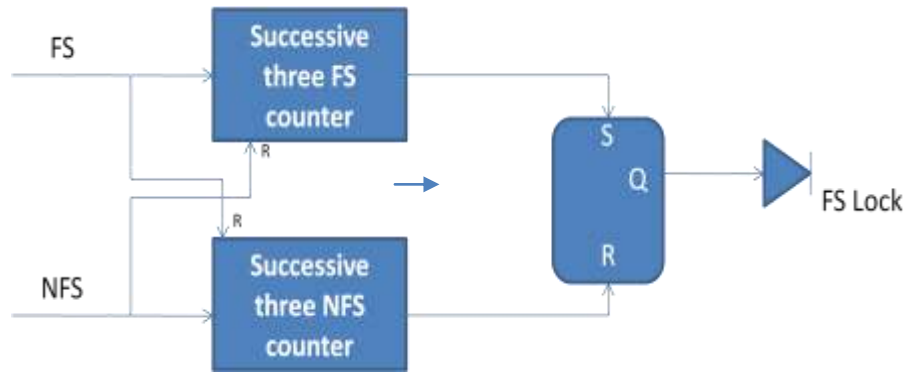
Figure 4 Flywheel lock logic

To generate frame timing in flywheel circuit, binary counter chain is used as shown in figure-5. These binary counters are configured to count in down count mode and parallel load mechanism. These counters are driven by system clock and the load input is given as binary count of frame length. Suppose, when frame sync pulse occurs, the counter chain is loaded with binary count value of frame length and further it is down countered when system clock occurs.
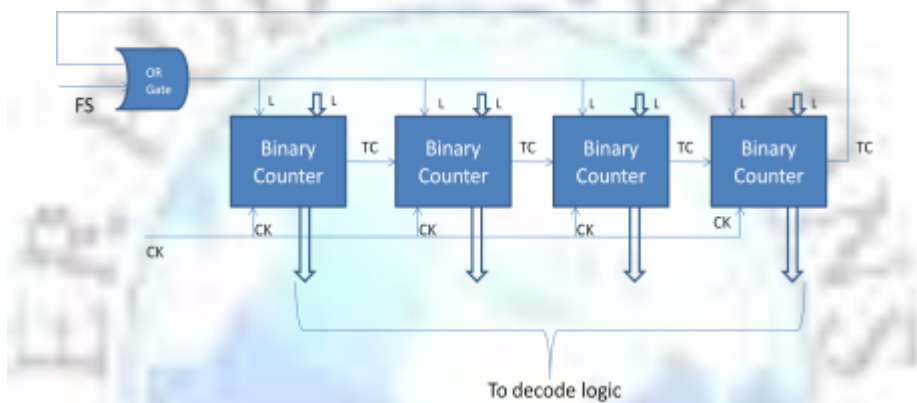
Figure 5 Flywheel frame length counter

When counter chain reaches the value of zero count, which means that frame timing is generated and the count chain gives terminal count TC. This terminal count is given to OR gate with FS pulse this is done because even if FS pulse is absent the frame timing will be generated.

Figure 6 Flywheel decoder logic

As shown in figure-6, the parallel count is given to the respective NOR and AND Gate logics and the signal is decoded. The output of the AND4 gate is the decoder pulse.

The decoder pulse sets the flip flop as shown in figure-7, prior to FS pattern arrival from satellite the decoder pulse occurs 10 bits earlier, thus the pulse sets the flip flop. This flip flop inverted output enables the binary counters during which it is set to the 148 bit length[8]. The length of 148 bits is chosen because FS length 128 bits plus 10bits plus 10bits, after frame synchronization is 148 bits. It is because, if FS pulse does not occurs after 10 bits then NFS will be

generated. This counter chain runs, if FS pulse occurs before 148 count it will reset the flip flop and fold back the counter, otherwise NO FS pulse will be generated.
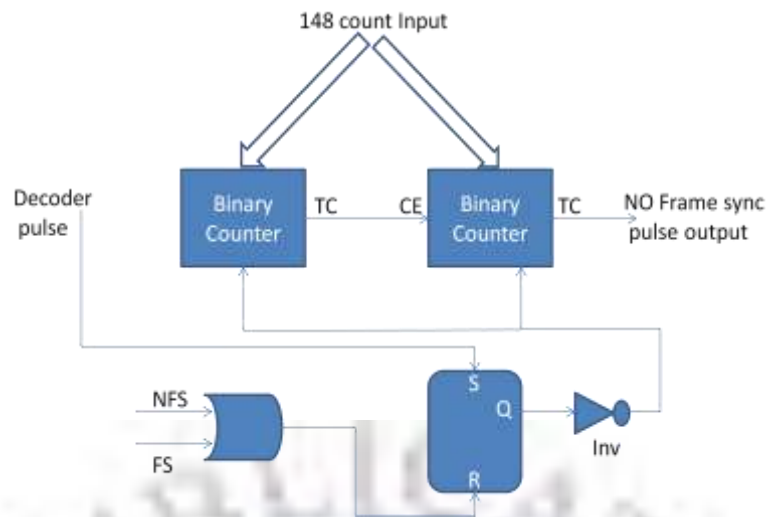

Figure 7   No Frame sync pulse generation logic

From figure-8, in this logic frame sync control signal has to be generated. The requirement is frame sync disable signal has to be generated after frame sync pulse generation and enable signal has to be restored prior to frame sync pattern occurrence. In the mean-time FS circuit will be disabled so that false frame synchronization will be avoided. Thus reliability of system is enhanced. The frame sync pulse through MUX will set the flip flop and the out of the flip flop will disable the frame sync circuit[9].
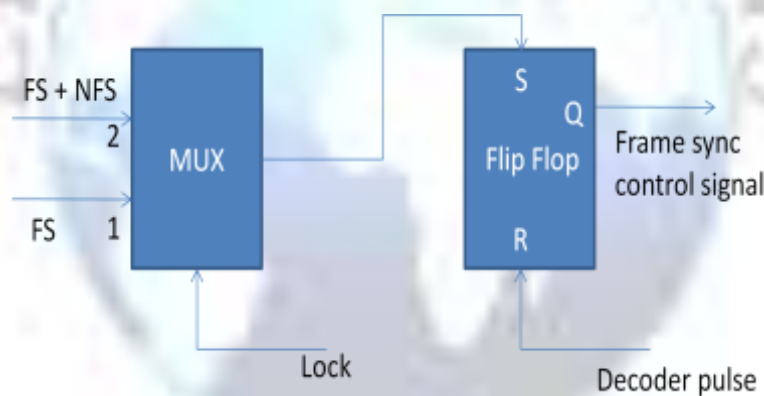

Figure 8 Flywheel frame sync circuit control generation

Decoder pulse will reset the flip flop and thus enables the frame sync circuit prior to frame sync occurrence. Once the system lock occurs, the operation changes slightly, i.e. lock signal selects the MUX to pass the signal FS + NFS to set the flip flop. This is because; in the absence of the FS pulse occurrence in lock status flywheel window generation will continue.

Automatic Frame Length Programming Logic

As shown in figure-9, the frame length counter is a up down counter to cater for all IRS satellite format lengths. The care is taken to accommodate longest format length. Initially, in the up count mode when FS pulse occurs it is reset (load-0). When second FS pulse occurs counter content indicates the format length corresponding to the IRS satellite data received. When third FS pulse occurs the situation is the same. Now with third frame sync pulse occurrence, circuit lock occurs and frame length binary value is loaded in the latch. This value is given back to frame length counter as input. With the third FS occurrence flip flop is set and its output configures the frame length counter to down count mode and also it enables the decoder and on passes FS pulses to other parts of the flywheel circuit. It stops the divide by 3 FS counter to give output. Thus the latch holds the frame length value.
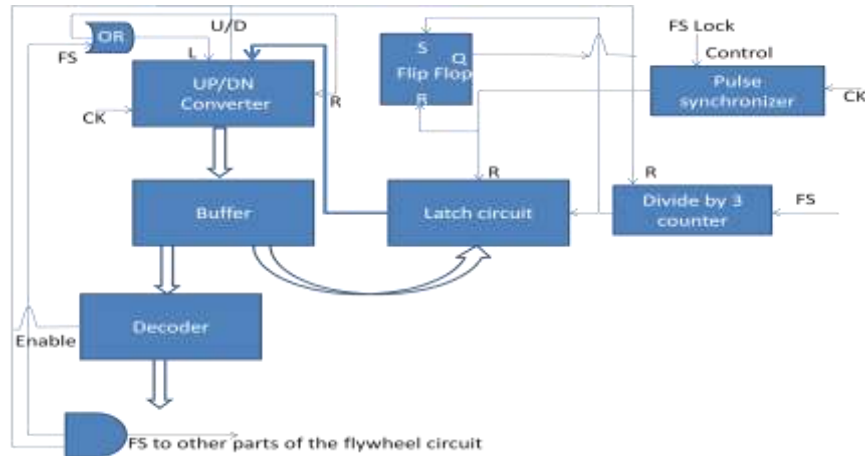
Figure 9 Automatic flywheel programming logic circuit

Hereafter, automatic circuit is programmed to frame lengths and flywheel operations which continue till the lock is lost. Once, lock is lost with the falling edge of that signal, one pulse is generated by pulse synchronizer to reset the flip flop, Latch and it enables divide by 3 FS counter to begin the whole operation once again. This process keeps on repeating. This is how automatic flywheel programming is achieved.

Conclusion

The design and Implementation of Automatic flywheel circuit is realized using CPLD's with high logical volume. The Flywheel circuit is one of the modules of the Real time BER validation system [6]. The other modules are Advanced Frame Synchronizer circuit[10] and BER Display logic This system works for all IRS satellite series whose Frame sync code is a PN sequence of $2^7 - 1$ i.e. 127 Bits. The circuit is tested using mentor graphic tools, implementation and programming is done using Xilinx ISE software. The system is installed in real-time satellite receive chain. The flywheel logic design is functioning perfectly and is regularly being used at Satellite Data Reception Station, NRSC.

Acknowledgement

References

[1]. Seymour Lip Schulz, "Theory of probability", McGraw Hill, 1981

[2]. Gruenberg E.L, "Handbook of Telemetry and Remote Control"1977

[3]. S.W.Golomb, "Digital Communications with space Applications, Prentice Hall 1964.

[4]. L.R.Button, D.E.Doods & A.G.Wacker "Digital Framing , Techniques for Satellite Channels" Technical study paper, 1983.

[5]. John G. Proakis, Digital Communications (4th Edition), McGraw-Hill, 2000.

[6]. R Srinivas ,P Naveen Kumar, P V V Subba Rao " Design and validation of online BER measurement of Satellite Data Channel for IRS Series Satellites

[7]. Bernard Sklar, Digital Communications: Fundamentals and Applications , (2ndEdition), Prentice Hall, 2001.

[8]. Heegard, A. J. King, S. Lovely, and T. J. Kolze, "Synchronization and error detection in a packetized data stream," Dec. 30, 1997.

[9]. R. B. Ward, "Acquisition of pseudo noise signal by sequential estimation,"IEEE Transactions Communications. Tech.,Vol1. COM-13, pp. 475–483, Dec.1965.

[10]. Srinivas R , Nityanandan L, Umadevi G, Rao PVVS, Kumar P N ; Advanced High Speed Parallell Frame Synchroniser for High Data Rate IRS Remote Sensing Satellite Series, in IEEE AEMC-Kolkatta-2012.