International Journal of Enhanced Research in Science Technology & Engineering,
Vol. 2 Issue 10, October-2013, pp: (54-59), Available online at: **www.erpublications.com**

Low power high speed bypassing based multipliers with modified adders for dsp applications

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Abstract: Braun multiplier is one of the parallel array multipliers, which is used for unsigned numbers multiplication. This paper presents different techniques for optimizing the multiplier in power and delay parameters. The dynamic power of a multiplier can be reduced by using bypassing techniques and delay can be reduced by replacing ripple carry adder in the last stage of full adders by optimized adders in different logics, Double pass transistor logic (DPL) and Transmission Gate (TG). Different logic style adders are designed and implemented in 0.13um CMOS technology and its functional parameters are compared and the best result is incorporated in the column bypassed Braun multiplier. And the new multiplier is used to implement a MAC unit which is more efficient.

Keywords : Double Pass transistor Logic (DPL), Modified Half Adder (MHA), Transmission Gate (TG), Carry-Look ahead Adder (CLA), Gate Diffusion Input (GDI) .

I. INTRODUCTION

Moore's law has predicted the growth rate of IC in VLSI industry. And its valid integration process is still on. Hence the number of transistors is shooting up and so is its power consumption .Similarly the processor speed has already crossed the GHz range and thus increases the demand for high speed arithmetic blocks .Thus many researches and studies are performed in the design and implementation of low power high speed arithmetic blocks.
In this paper an improved version of array multiplier with bypassing techniques and modified adder module is implemented for a low power high speed MAC. The adder circuits are optimized for delay in different logics like TG, DPL which are among the faster logic design for adders.

Braun multiplier [1] is a parallel array multiplier [2] which is usually used for unsigned and Two's complement signed multiplication. A conventional Braun multiplier contains n (n-1) number of full adders and n^2 AND gates. The hardware increases exponentially as number of bits increases, thus larger area. This is one of the drawbacks of conventional array multipliers, hence to reduce the power consumption we incorporate bypassing techniques in Braun multiplier. Delay of the multiplier depends on the delay of the full adders used in the design.

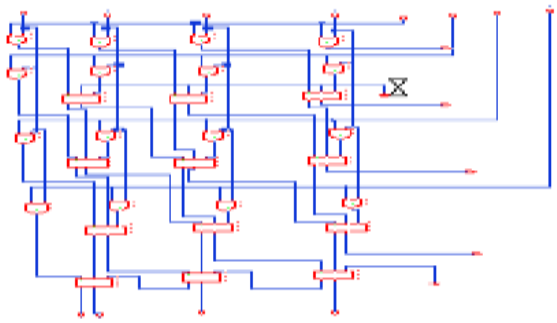

Figure 1.4x4 Braun multiplier

A 4x4 Braun multiplier consist of 3 rows of carry save adder and there are 3 full adders in each row .The last row is a ripple carry adder for carry propagation.

The introduction of the paper should explain the nature of the problem, previous work, purpose, and the contribution of the paper. The contents of each section may be provided to understand easily about the paper. (12)

II. LOW POWER COLUMN BYPASSING TECHNIQUE

Parallel array multipliers [3] are widely used in DSP applications. Hence its power consumption should be reduced to make it compliable for low power applications. There are several methods to reduce dynamic and static power of an array multiplier such as, reducing switching activities, interchanging dynamic operands, using partial guarded computation. Reduction of power by modifying architecture method can be achieved by row/column bypassing. Here in this paper column bypassing [4] is used, which reduces the switching activities by bypassing the result to next level.

In column bypassing technique [6], if any one of the bit in the (j+1) th column is 0 then the addition operation to be performed in that column can be bypassed. All a_jb_i partial products will be zero. The modified full adder in column bypassing is less complex than the row bypassing. Column bypassing require only two tri-state buffers and one 2:1mux in order to skip the FA cell in columns of zero bits.. It also reduce the hardware area when compared to row bypassing technique. For a Braun multiplier, there are only two inputs for each FA in the first row (i.e., row 0). Therefore, when a_j is 0, the two input of FA0 (j) are disabled, and thus it output carry bit which will be the same. Therefore, all three inputs of FA1 (j) are fixed, which prohibit its output from changing.

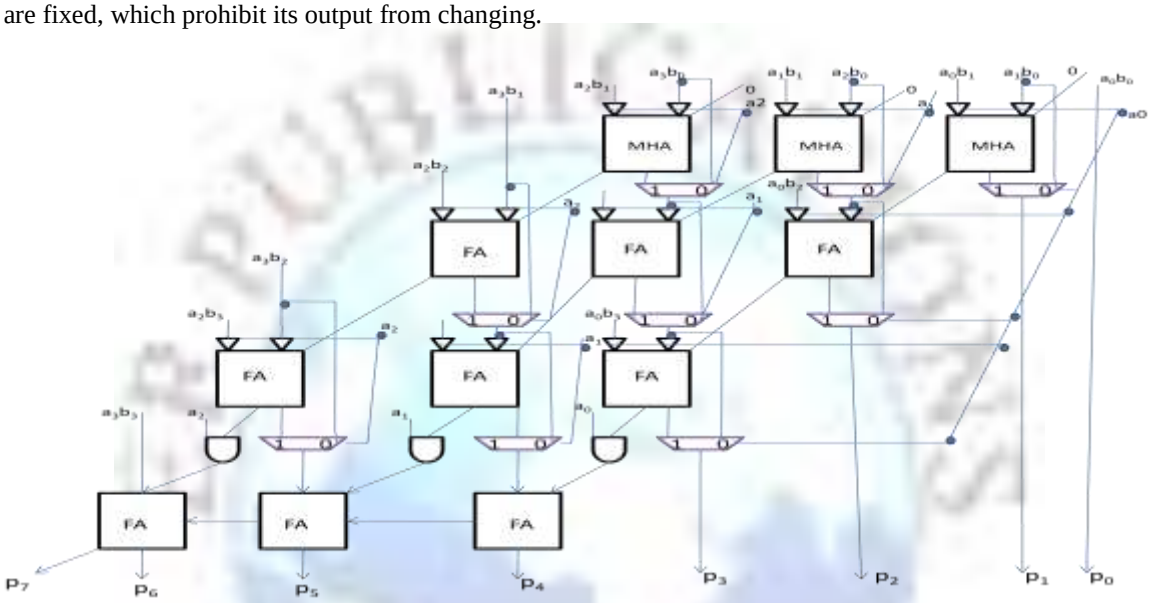

Figure 2: Braun multiplier with column bypassing.

Figure 2 shows the components and connection between each component in a column bypassing Braun multiplier. The components used in the Braun multiplier with column bypassing are full adder, AND gate, tri-state buffer and a multiplexer. The first row of adders has only two inputs hence can be considered as half adders. In the above architecture we have 3 Modified Half Adders (MHA). Figure 2 shows the schematic of column bypassing based 4x4 array multiplier.

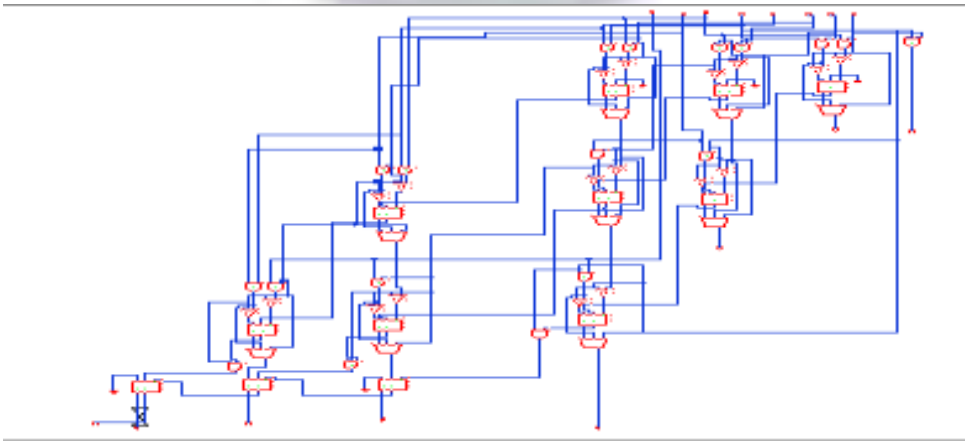

Figure 3: Braun multiplier with column bypassing

III. MODIFIED FULL ADDERS IN DIFFERENT LOGIC STYLES

Adders are the most essential and indispensible arithmetic blocks in multipliers, ALU and other computational applications. Hence the power consumption and delay are very crucial parameters. There is no ideal full adder cell that can be used in all types of applications. Different logic styles are used for their best feature depending on the type of application for which it is utilized.

The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. Power consumption and speed are two important but conflicting design aspects. A Braun multiplier consists of 3 rows of carry save adder and 1 row of ripple carry adder. In order to reduce time delay the last row of ripple carry adder can be replaced by carry-lookahead adder or Kogg's stone adder. But for large numbers this is no longer the case, because even when carry look-ahead is implemented, the distances that signals have to travel on the chip increase in proportion to *n*, and propagation delays[5] increase at the same rate. In this paper we replace ripple carry adder with carry –lookahead adder and it is optimized. A comparative study has been done on this adder with different logics like DPL [7], TG (Transmission gates) for

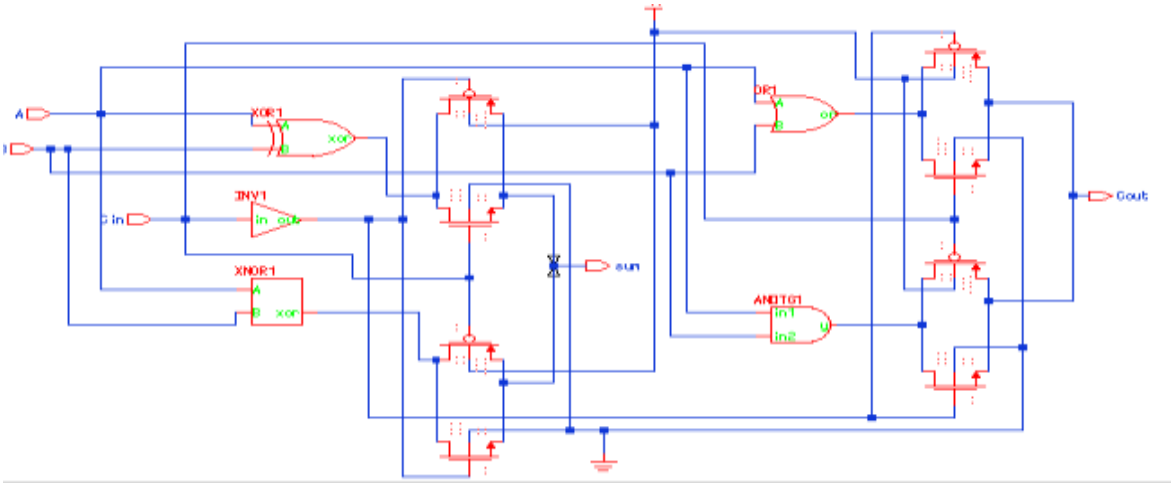

Figure 4:. 1-bit Transmission gate full adder

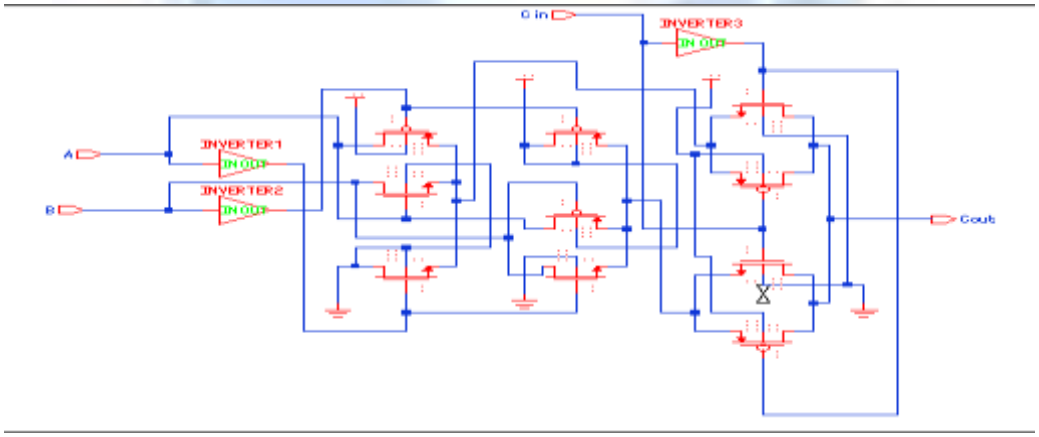

Figure 5:. 1-bit DPL full adder sum circuit.

IV. MAC ARCHITECTURE

Most of digital signal processing (DSP) applications, the critical operations usually involve many multiplications and accumulations. So, for a real-time signal processing, a high speed and high throughput Multiplier- Accumulator (MAC) is always a key to achieve a better performance digital signal processing system. In the last few years, the main consideration of MAC design is to enhance its speed and to reduce its power. This is because speed and throughput rate is always the great concern of digital signal processing system. In the proposed MAC structure we have a 8 bit adder, proposed multiplier and an accumulator unit . The accumulator units consist of a PIPO register with D flip-flop and a Carry Lookahead adder

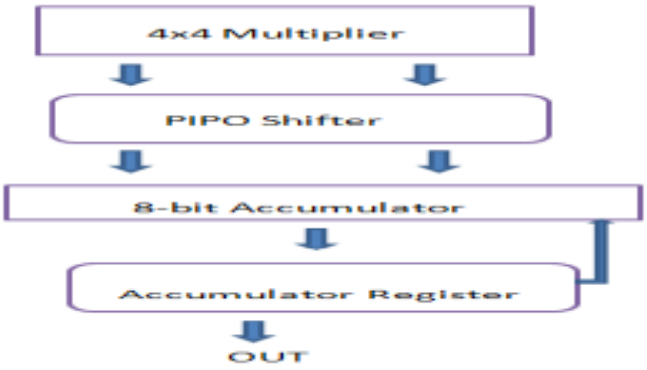

Figure 6: MAC Architecture

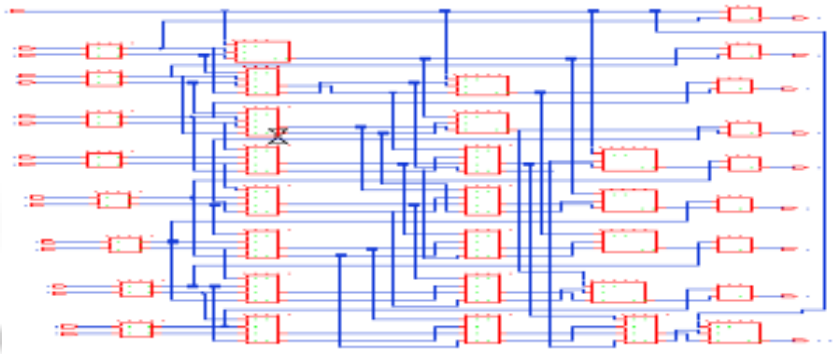

Figure 7. 8 bit Carry Look-Ahead Adder

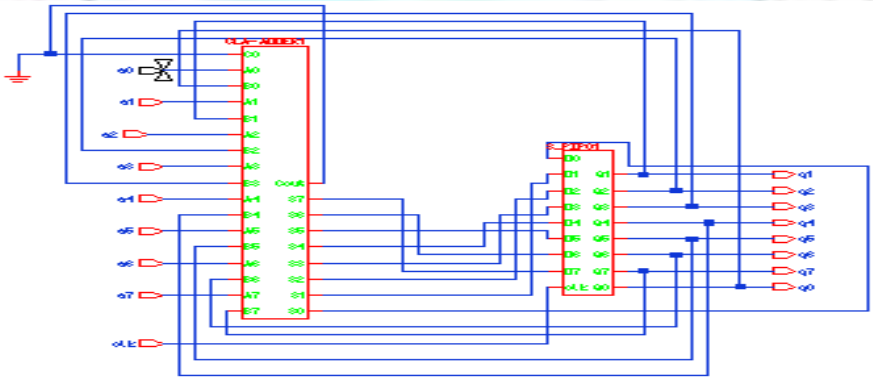

Figure 8. 8 bit Accumulator

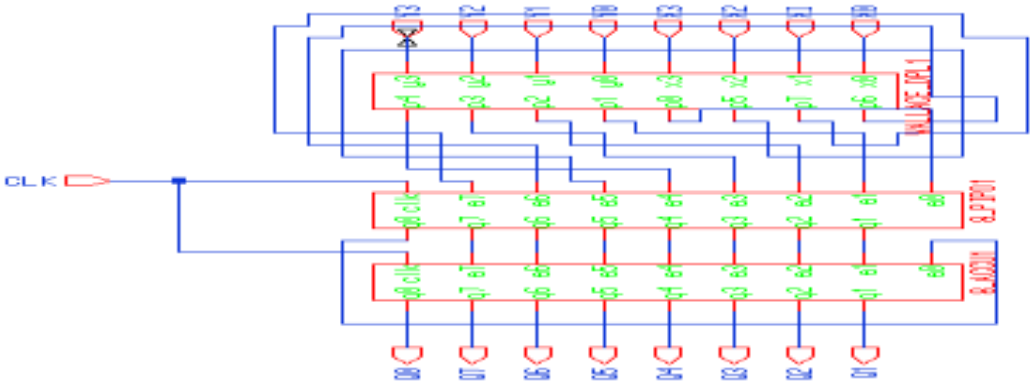

Figure 9: 8-bit MAC

V. RESULTS AND DISCUSSIONS

Braun multiplier with column bypassing technique is implemented in which the last stage of ripple carry adder is replaced by carry-look ahead adder (CLA). Carry-lookahead adder is designed in DPL and TG logics for optimization of delay. The optimized multiplier is used to implement a high speed low power MAC unit. Design and implementation of the multiplier is done in 0.18um CMOS technology. The analysis has been carried out on the proposed multipliers by performing simulations on Mentor graphics. The results are compared with existing Braun multiplier. Simulations are performed for 4x4 bit multipliers at 0.8 to 1.2V and at a frequency of 200 MHz it has been observed that DPL bypassing based multiplier logic has lowest PDP it can be used for high speed and low power digital circuit very efficiently.
The improved array multiplier is then compared to Wallace tree multiplier to analyze the degree of improvement it has acquired.

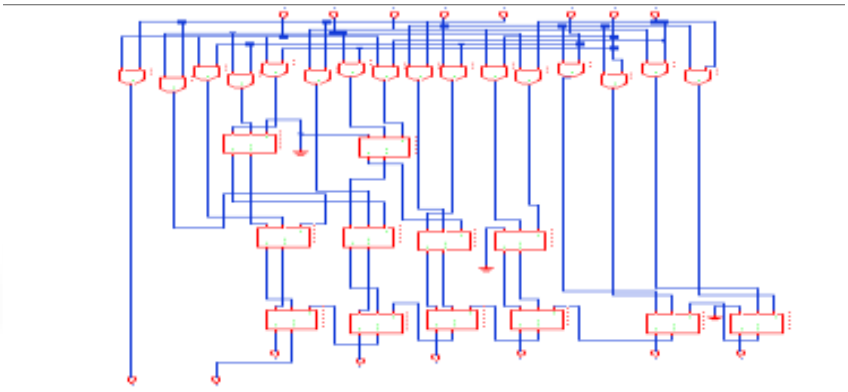

Figure 12: 8-bit Wallace tree Multiplier

TABLE 1: Comparative Analysis Of Different Adders

LOGIC STYLE	POWER(nW)	No.of Transistors
CMOS	5.883	28
DPL	2.1063	26
TG	9.805	20

TABLE 2: Comparative Analysis Of Different Array Multipliers

MULTIPLIER	POWER	DELAY
TG	1.32	$1.99x10^{3}$ pS
DPL	0.174	$2.109x10^{3}$ pS
Bypass TG	$1.0082X10^{-3}$	158.80 pS
Bypass DPL	683.53 $80X10^{-6}$	152.6pS
WALLACE	260.37X 10^{-9}	23.662pS

TABLE 3: Comparative Analysis Of Different Mac Units

MAC	POWER	DELAY
DPL	341.980uW	2.109 uS
Bypass DPL	228.592uW	0.9991uS
WALLACE	257.55uW	1.0002uS

VI. CONCLUSION

Optimized parallel array multiplier by incorporating bypassing technique for power reduction. Reduced delay by implementing high speed adders in multiplier using TG and DPL. The final simulation states that DPL adder multiplier with output MUX logic and bypassing technique for power reduction it almost got in par with Wallace Tree multiplier Thus our proposed model of multiplier with bypassing and DPL adder is better for DSP applications, like MAC unit than the conventional parallel array multipliers.

Even though the technology used in this paper is 130nm it is sufficient for analysis and comparison purpose the same can be extended for state of art technology. This modification can be extended for high-speed low-power multipliers, by taking this alternative logic structure and trying on new realizations for the constituent logic blocks (XOR/XNOR, AND, OR and MUX cells).And another novel logic called Gate Diffusion Input (GDI) for full adders.

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