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Fate of MOSFET anatomy implementing double gate to dwindle the short channel aspects and drain induced barrier lowering

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Abstract: This paper focus on the fate of the DG MOSFET, by comparative and analytic study of different phases of double gate which dwindle the SCE and DIBL. We can easily recognize in current era that in which pace transistor has diminished in its size in same rate its manufacturing has increased. A drop off in the size of MOSFET has adversely affected its electrical attributes. Collectively 2D NEGF, NS-DG MOSFET and DG CNFET are analyzed. Eternal trawl are going on ATLAS™. We accentuate in this work piece glories of next step future DCNFET, it will accommodate to midget size by the use of nano wire.

Keywords: Short chanel effect, Double gate MOSFET, drain induced barrier lowering, 2D NEGF, NS-DG MOSFET and double gate carbon nano tube FET.

INTRODUCTION

In the contemporary world, we need the miniature MOSFET. The researchers are continuously going on for this purpose. The navel of the microprocessor is latches and again the bare bones of the latches are the MOSFET. Latches are the memory storing cells made up of the logics and upshot of all is the Metal Oxide Field Effect Transistor. If we need to abridge the size of the microprocessor, we will have to allay the size of latches then undoubtedly MOSFET. It is very much clear that as per the size of MOSFET decreases, directly affect the current technology.

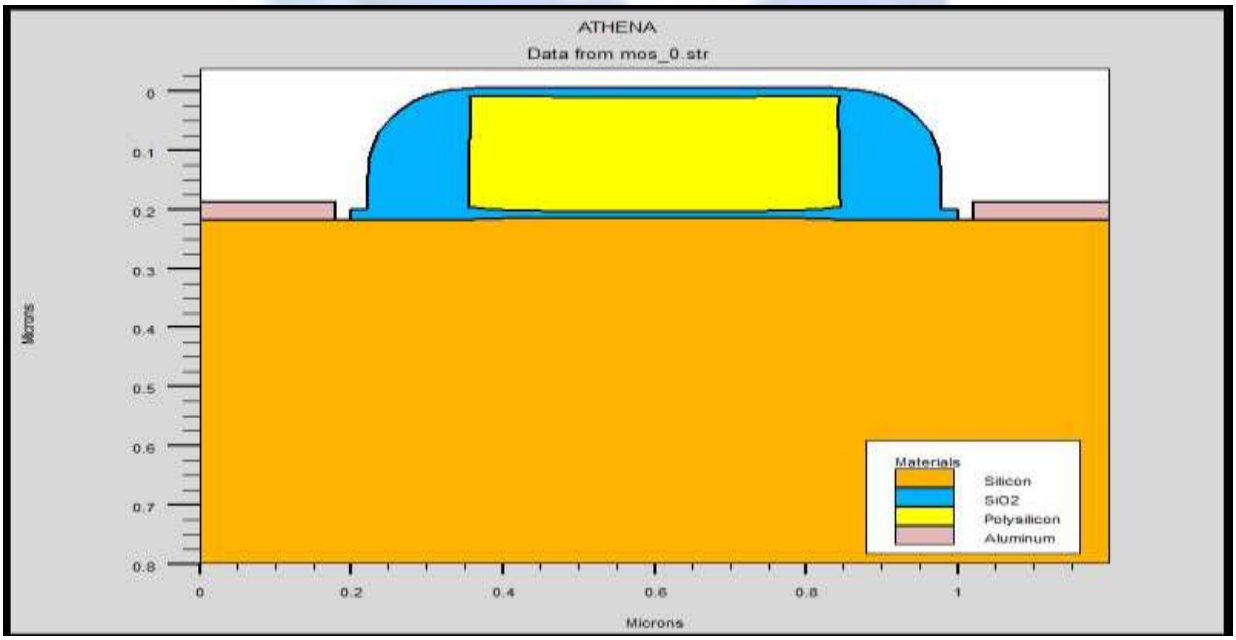
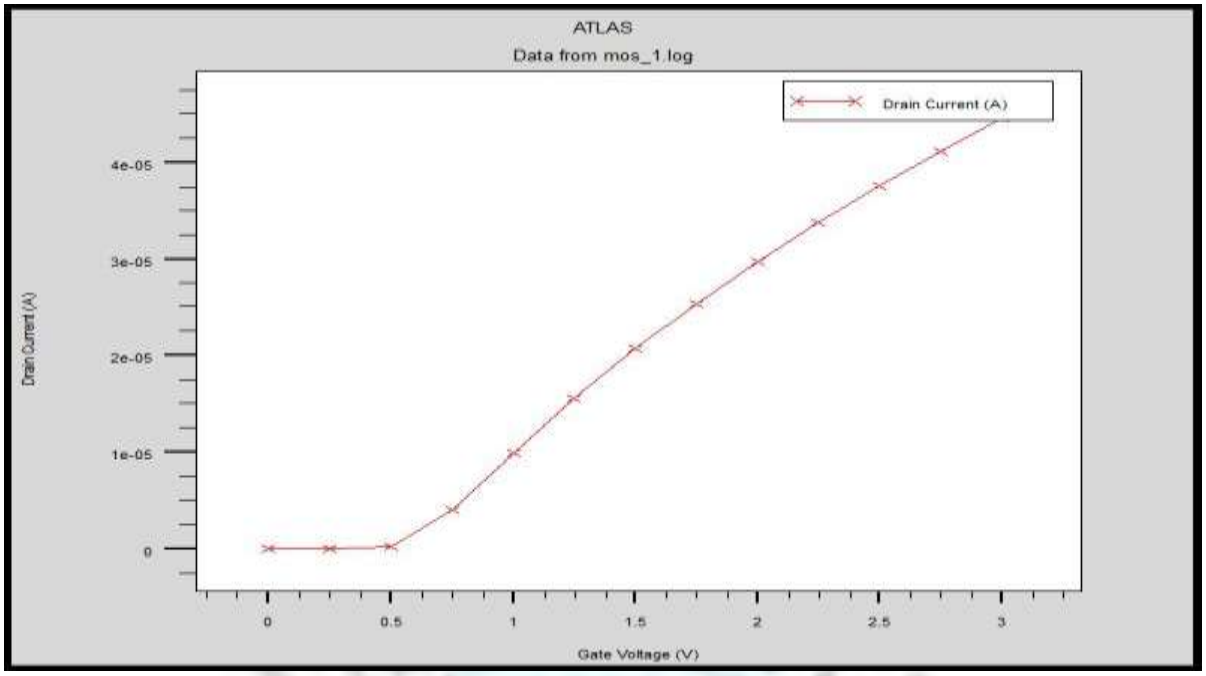


Figure 1: Rudimentary of a MOSFET on ATLAS

The fig (1) is drawn by the ATLAS TCAD design simulation software, the drain current and gate voltage is optimized shown in fig(2).



Modeling of PV System

Figure 2: Drain current verses gate voltage of the MOSFET on ATLAS

Now in recent microprocessors, more than 2 billion MOSFETs are in use. So abating the area of that much MOSFETs causes several problems, like switching [2], SCE and DIBL. If we create them in petite way then switching condition will become worst. In the current paper, we present one of the best comparative and analytic panaceas, which will pay a way to resize without disturbing the attributes.

I. MOORE, G.E. CRAMMING'S SPECULATION

In the year 1965, Goorden Moore render the behavior of transistor density, it will twofold the density of transistor in 18 years [3].

In 1974, asset of scaling [4] was put in spotlight by Dennard and crony. They brought up that the switching speed will boost by a factor K. If scaling of the device by same factor K also degrade the power dissipation by K^2 and power delay product increase by K^3. It is superseded by the VLSI industry until year 2005.A cherishing thing is short channel effects, which evolves due to reduction in the anatomy of MOSFET means affecting the separation between drain and source, which is from 30 nm to 20 nm, there are many flaws enter in list and one of them is DIBL (drain induced barrier lowering).It creates depreciation in sub threshold which increase the leakage current finally dead horse in switching speed and other parameters.

$$\varnothing = {}^{-\Delta f}/_{2f} \quad [V_{DD} - V_t] \qquad (1)$$

Where f is max operating frequency; $\varnothing$ is IDBL shows by the eq(1).

II. DGMOSFET PORTFOLIO: 2D NEGF APPROACH

Simulation of a novel nanoscale DG-MOSFET: 2D NEGF Approach was presented by Nima A. Dehdashti et al in year 2007[5], paper focus on electrical attributes of a reminiscence NS DG-MOSFET) by a full Quantum Mechanical simulation framework, embrace Non-Equilibrium Green's Function (NEGF) surmounted by Poisson's Equation. Quantum transport equations are carry off 2-D by iterative NEGF method to gain the charge density. Poisson's equation was solved in absolute territory of simulation to obtain potential track record. The resounding drain current was deliberated by Launder formula

$$I = {}^{2Q}/_{H} \int dE\, T_{sd}(E) \left(f_s(E) - f_d(E) \right) \qquad (2)$$

in the above eq(2): f_s , f_d are the Fermi functions at source and drain junctions respectively. The plots on I_D versus V_{gs} is shown in the fig(3) [6].

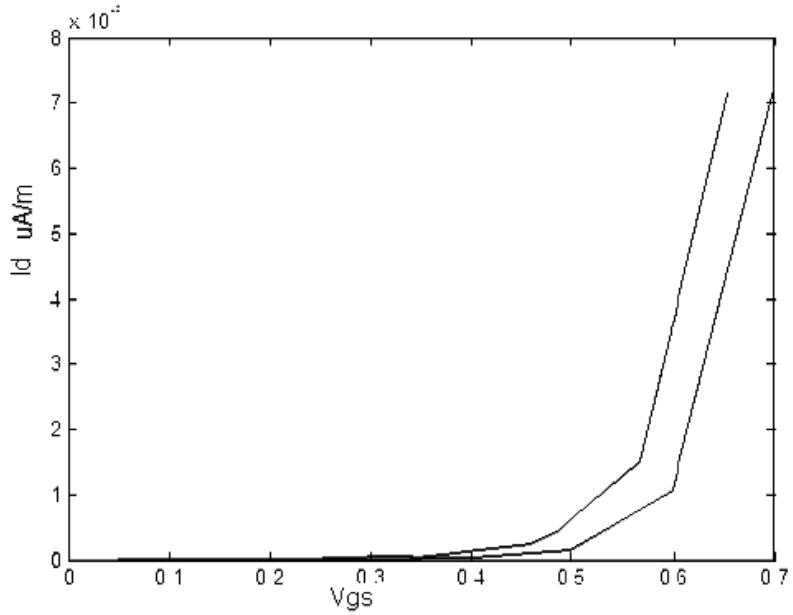


Figure 3: I_D versus V_{gs} for different V_{ds} parameters

III. RENAISSANCE IN NS-DG MOSFET

Sushanta Kumar Mohapatra et al focused on the pyrotechnics of Double Gate Metal Oxide Semiconductor Field Effect Transistor in year 2012 with contrasting channel and gate engineering. Five anatomies were analyzed by keeping enduring channel length. The short channel constraint like Sub threshold Swing, Transconductance, Electric Field, Surface Potential, Total Current Density, Output Conductance were compiled and compared among Fully Doped, Un-Doped, Graded Channel, Dual Insulator and Gate Stack DG-MOSFETs. The simulation and parameter extraction had been done by using the commercially available device simulation software ATLAS™, the rudimentary and characteristic is shown by the fig (4) and fig (5) respectively[7].

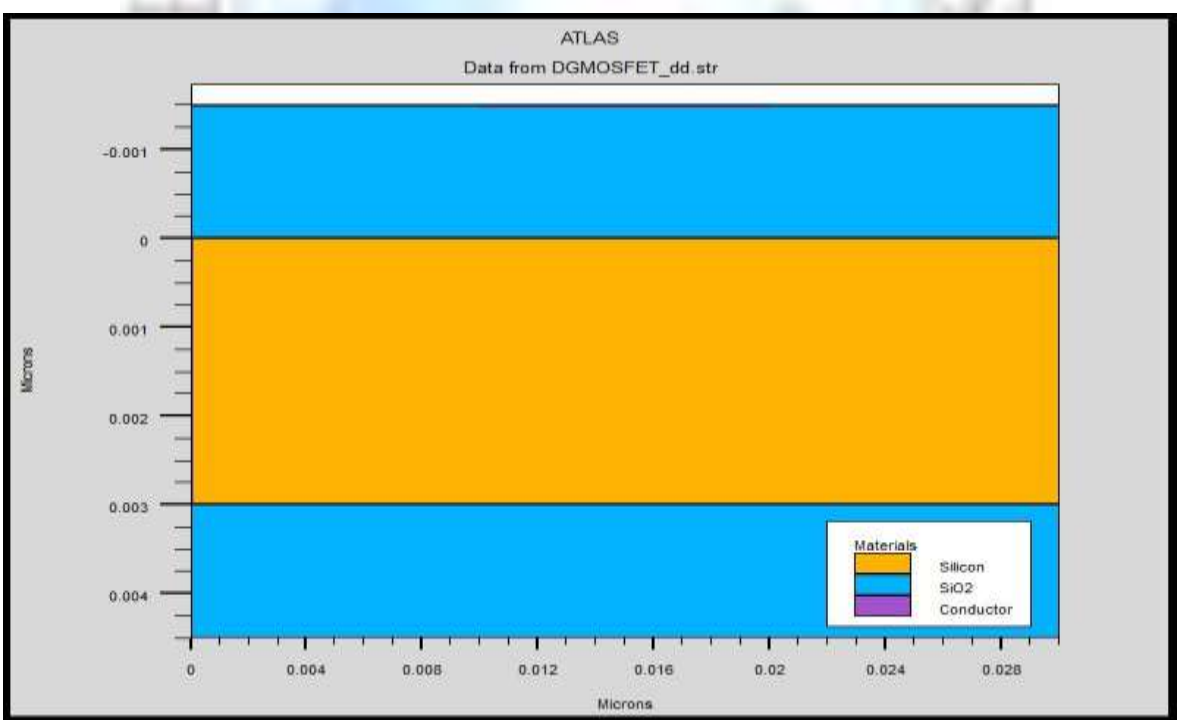


Figure 4: Rudimentary of a DG-MOSFET on ATLAS.

Pao-Sab's integral can be given as:

$$I_{ds}=\mu \, {}^{W}/_{L} \int_{0}^{V_{ds}} q_i \, (v)dv \qquad (3)$$

where q_i is the total mobile charge/unit area considering both channel. Further we get the drain current in saturation region [8] as:

$$I_{ds}=\frac{\mu W/L\,\epsilon_i}{t_i}\left[\left(V_{gs}-V_t\right)^2-\frac{8\epsilon_{si}}{\epsilon_i}\frac{t_i}{t_{si}}\frac{k^2}{q^2}T^2e^{\frac{q(V_{gs}-V_t-V_{ds})}{kT}}\right] \quad (4)$$

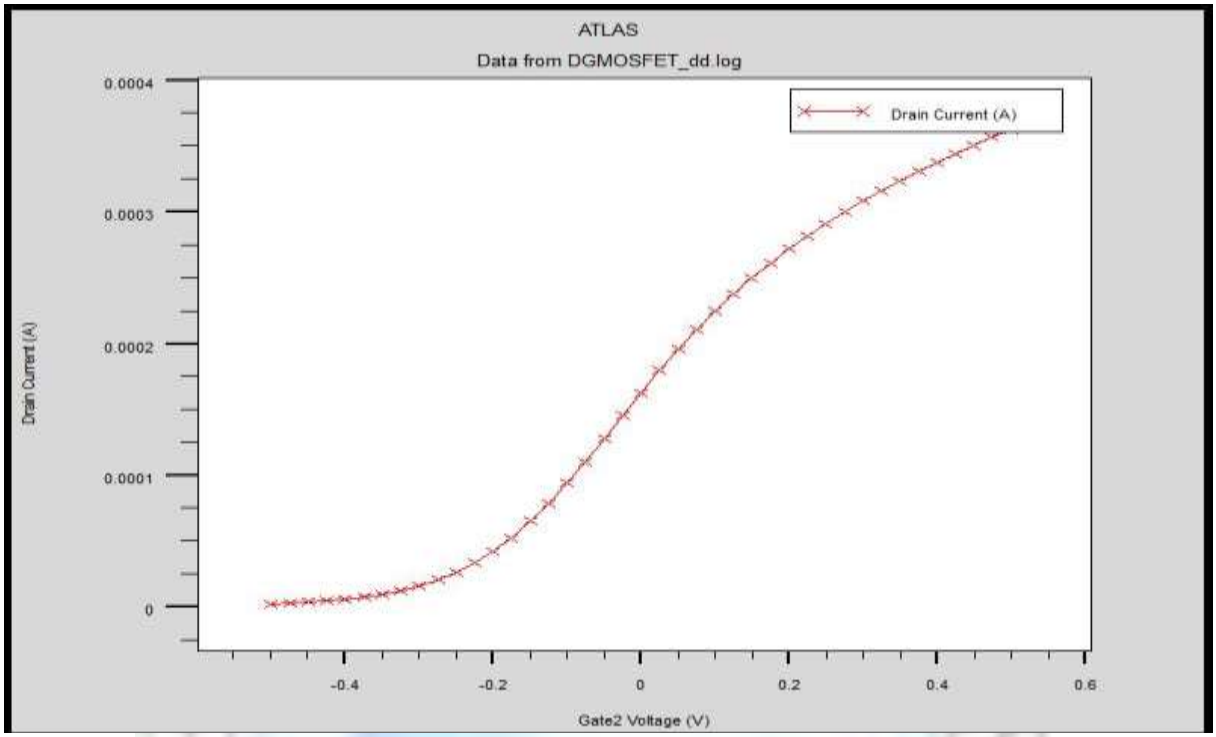


Figure 5: Drain current verses gate 2 voltage of the DG-MOSFET on ATLAS.

Threshold voltage (V_{th}) is also a vital constraint for higher on state current which boost the circuit speed. The V_{th} is derived by calculating the maximum slope of the drain-gate curve, establishing the intercept with the x-axis after that subtracting half of the didactic drain bias. The drain current and gate voltage with different profile is shown in fig (6).

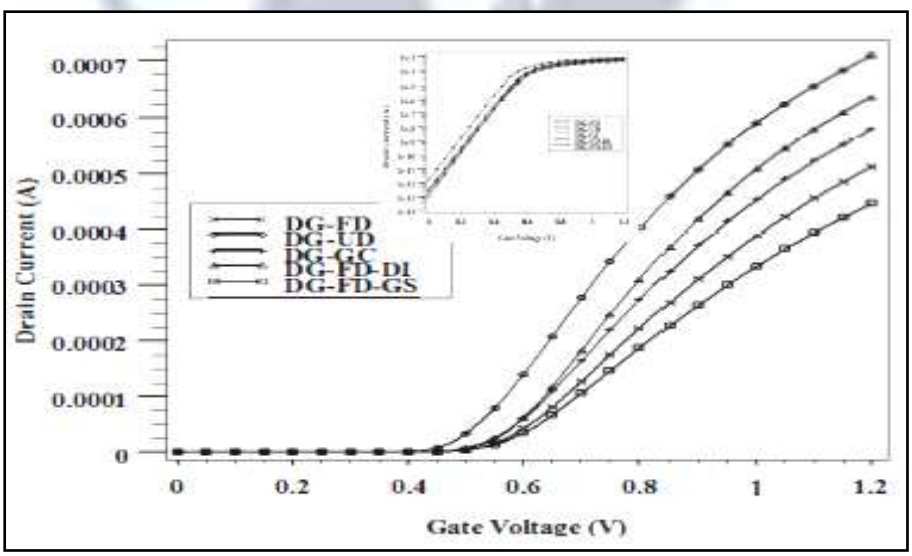


Figure 6: Outlook of Drain Current (I_D) with Voltage (V_{GS}) at V_{DS} =0.1 V

IV. CONSCIOUSNESS OF DG-CNFET

The double gate (DG) MOSFETs are electro-statically unhoped-for others than a single gate MOSFET and empower for supplementary gate length scaling, nanotechnology has accomplished a enormous giant step in fabrication of divergent devices at nanometer like molecular diodes and Carbon Nanotube field effect transistors (CNFETs). This has provided revolutionary scope for VLSI circuits to pull off continues cost cutback and pyrotechnics upswing in post-silicon-based-CMOS-technology. Carbon Nanotube based FET devices are getting fourfold emphasis today due to enhanced I-V characteristics and high channel mobility are perceptive standby for morrow semiconductor devices. Mr. S.S. Chopade and friend focused on consciousness of DG-CNFET in year 2013. The paper suggested the design of DG CNFET by altering material like polysilicon with CN-tube at 20 nm technology. It was observed that DG CNFET had dench monpoly on leakage current & ratio I_{ON}/I_{0FF} of DG-CNFET is 6.05 times greater than the DGMOSFET, fig(7) & fig(8) showing 2D anatomy and characteristic of I_{DS} versus V_{DS} respectively [9].

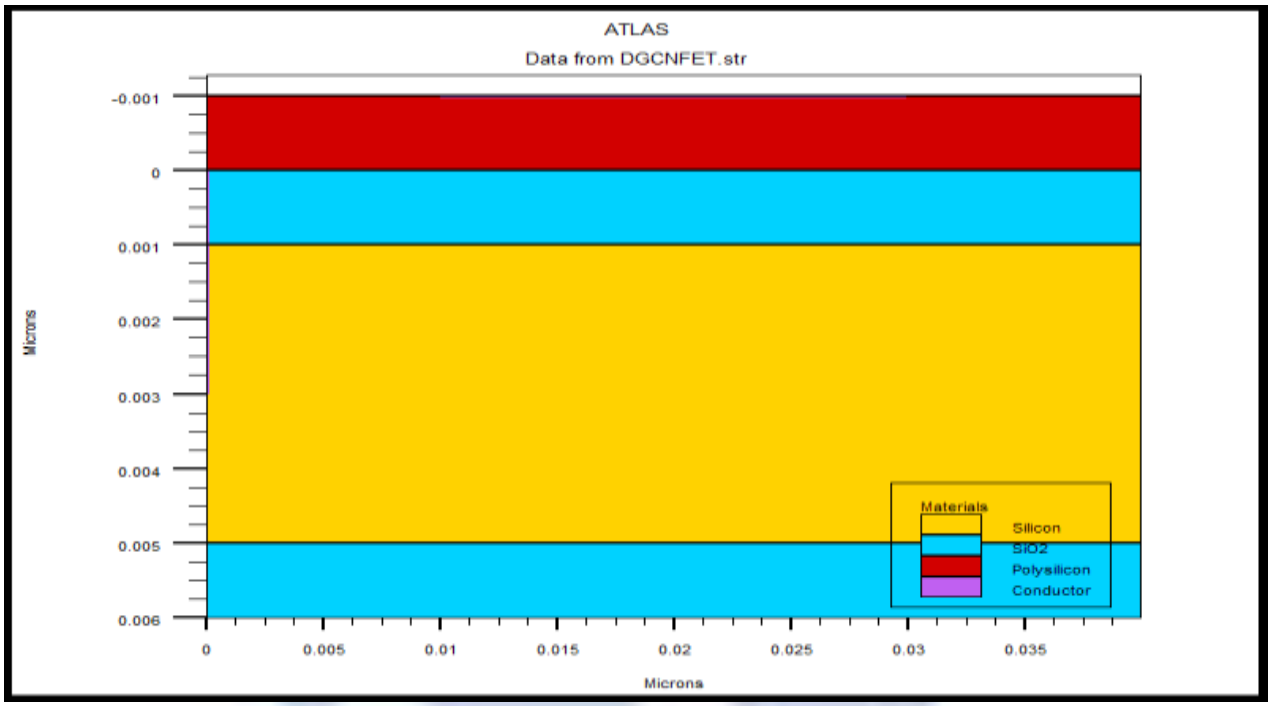


Figure 7: 2 D Device anatomy of DG CNFET on ATLAS.

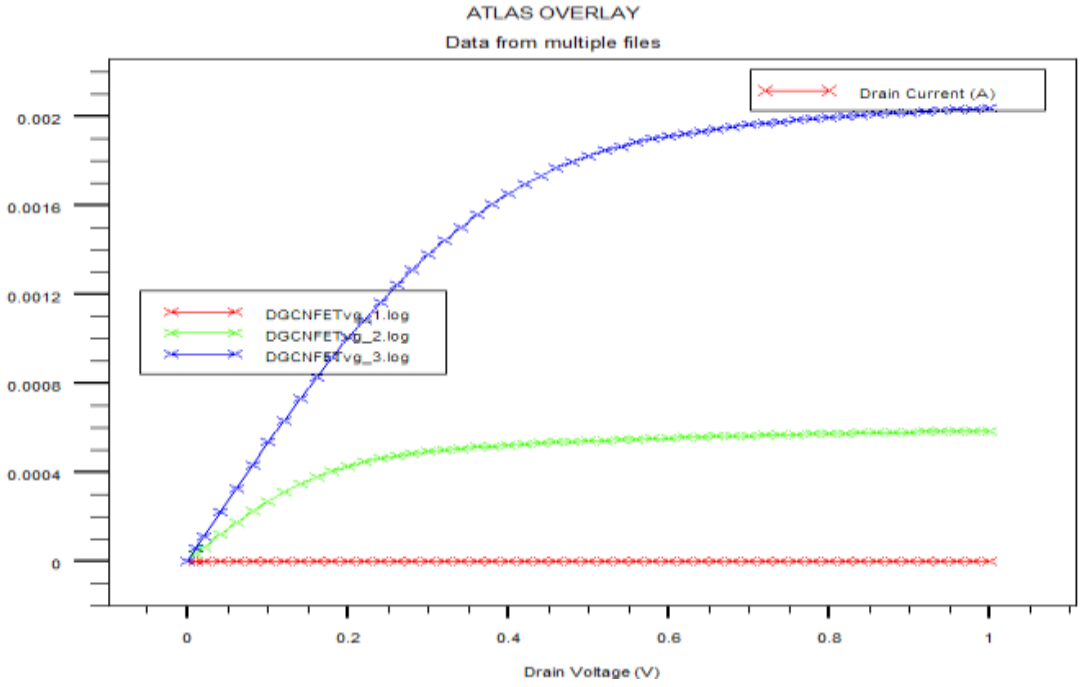


Figure 8: I_{DS} versus V_{DS} : restraint of polysiliocn to CN-tube restraint for V_{GS}=0, V_{GS}=0.5 & V_{GS}=1.0v

V. RESULT

Threshold voltage V_T is calculated when V_{DD} equal to 0.1Volt while V_g is varied from 0.0 Volt to 1.0 Volt by a factor of 0.1 V. VT is 0.166 Volt for VDD =0.1 Volt for Double gate CNFET. Thus, it is necessary to optimize some relative factor of VT such as doping level, thickness and the value of hole and electron mobility of Polysilicon.

The extracted of V_T, I_{OFF} & I_{ON} are
V_T is 0.166 Volt for VDD =0.1 Volt
I_{OFF} is 18.73 nA for VDD = 0.1 Volt
ION is 533 µAfor VDD = 0.1 Volt for Double gate CNFET.

Rudimentary of both, DG MOSFET and DG CNFET has designed on silvaco TCAD ATLAS tool at 20 nm and results has presented. The comparative results are shown in table 1 for V_T,

TABLE I: DATA OF DG MOSFET & DG CNFET WITH 20NM SCALE

V_{DD}=0.1V	V_T(V)	Sub V_t Slope (mv/dec)	I_{on} (µA)	I_{off} (µA)	I_{on}/ I_{off}
DG MOSFET	0.106	63.44	158.3	4.15	3.09×10^3
DG DCNFET	0.166	65.22	22	533	18.73×10^3

From table we find that DG CNFET is having a control over current as I_{OFF} is down from 158.3 nA to 18.73nA. The ION/ IOFF Ratio have enhanced by 6.06 times (606%) by using DG CNFET.

CONCLUSION

Our whole research work is based on DG MOSFET comparative and analytic study of different phases, which talks about implementing theories and equations to work and orchestrate it. We are saying so, as we are conversing that ULSI industries, which are prolific today, will take a sound epoch to pull off the spurt level of DG MOSFET. Even we have further vision that from MOSFET to DGCNFET an innovative turn of the century will blossom in form of nanotechnology which will be unquestioning go through the roof by every year. DG CNFET will embellish the enhancement of ON-OFF current ratio by 6.06 times

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