

Study of Static Power of Clocked Pair Shared Flip Flop For Low Power Clocking System

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Abstract: In the past, the major issue of the VLSI designer were area, cost, performance, and reliability; power consideration was mostly of only inferior importance. But over the last few years power in the circuit is the major problem now days which is being faced by the very large scale integration industries. The power dissipation in any circuit is usually take place by the clocking system which includes the clock distribution system and sequential elements (flip flops and latches) in it. The amount of power dissipation by any clock distribution system and sequential circuit in any chip is about of 30% to 60% of the total chip power dissipation by the circuit. Clock is the most important signal present in the chip. Clock signals are synchronizing signals which provide timing references for computation of any work in synchronous digital systems. In this paper the static power of the clocked pair shared flip flop of the clocking system is surveyed with the help of the H spice software.

I. INTRODUCTION

In the past, the major importance's given by the VLSI designer were area, cost, performance and reliability; the field of power was mostly considered of only inferior importance. But in recent years, however, this is getting change and power is being given similar importance same as the area and the speed. There are several factors which focus light towards the power factor of the chip or design. In high-speed implementation of any circuit and complex functionality applications with low power consumption of the circuit is of critical concern. The art of the power analysis and its optimization of the integrated circuits is very important in the chip designing procedure. The need of the low power chips and the system are driven importance by both in the business and the technical fields. There are generally four sources of power dissipation in digital CMOS circuits. They are: switching (or dynamic) power, short-circuit power, leakage power, and static power. These are summarized in the following:

$$P_{avg} = P_{switching} + P_{short\ circuit} + P_{leakage} + P_{static} = \alpha C_L V_{dd}^2 f + I_{sc} V_{dd} + I_{leak} V_{dd} + I_{static} V_{dd}$$

The switching power $P_{switching}$ consists of the activity factor α , or the average number of transitions for a circuit node per clock cycle, the load capacitance C_L switched, and the power supply voltage V_{dd} which is mostly in the cases the voltage is always equal to the supply voltage ($V=V_{dd}$). The short-circuit power is controlled by the current that flows between V_{dd} and ground I_{sc} . This current flows in static CMOS logic when both the P_{pullup} and $N_{pulldown}$ networks are on simultaneously during an output transition. I_{leak} the main component of the leakage power is current due to leakage through reverse-biased PN junctions and sub threshold conduction of MOSFETs. Finally, static power is due to designed current sources, like biasing networks for linear amplifiers, whose current sums to I_{static} .

Here clocking system is the main point in the chip configuration [1]. The clock network constitutes one of the most important segment of a synchronous VLSI chip as it can significantly influence the speed, area, and power dissipation of the system. The carefully design of the clocking system is generally a neglected in the design process. The reason of this is that the older chip had higher tolerance to the change in the clock signal and had less execution timing requirements. However with the increase in the demand of the high speed operation the design of the clocking system has being very important concern in the chip. The system timing specifications are executed using clocking system.

There are large numbers of methods available to reduce the energy and power consumption of a chip in a circuit. There are many approaches which focus on circuit and its application specific techniques, There are techniques for power reduction that are non-application specific, which includes widely popular techniques such as voltage scaling, frequency scaling and leakage power reduction [2]. Voltage scaling combined with frequency scaling is very popular because reducing the supply voltage of a CMOS circuit lowers the active and leakage power polynomials, while only reducing the frequency linearly. The dynamic power loss has been dominant culprit in the past, static power loss has become a considerable contributor to power consumption in nanoscale technologies due to leakage currents. One of the main causes of static power loss is leakage currents. There are wide varieties of techniques designed to reduce leakage

currents as the power dissipation by this has become one of the most dominant factors in total power consumption and is a challenge for the VLSI designers

II. Survey of Low Power Clocking System

Flip-Flops are the basic elements for storing data and they are the fundamental building blocks for all sequential circuits. In Flip-flops their content change only either at the rising or at falling edge of the enable signal. But, after the rising or falling edge of the enable signal, the flip-flop's content remains constant even if the input data changes. The part of the clock energy is consumed by the internal clock buffer to control the transmission gates unnecessarily. CDMFF and CCFF both have large clocked transistors. For example, CDMFF used 15 clocked loads and CCFF used 14 clocked transistors. In respect to this, conditional data mapping flip-flop used only 7 clocked transistors, which resulting in about 50% reduction in the number of clocked transistors load, so due to this CDMFF used less power than CCFF and CDMFF. This result illustrate that the by reducing clocked loads numbers help in achieving low power. Since CDMFF is better in performance than CCFF and CDMFF in respect of power consumption [3].

CDMFF ha less number of clocked loads but it has redundant clocking in it and it has floating node as a drawback. To result in efficient and error free implementation of low power register element, a Clocked Pair Shared flip-flop (CPSFF) is proposed. In this circuit of clocked-pair-shared flip-flop, a clocked pair (N3, N4) is shared by first and second stage of the latching part as which is shown in figure 1 below [4].

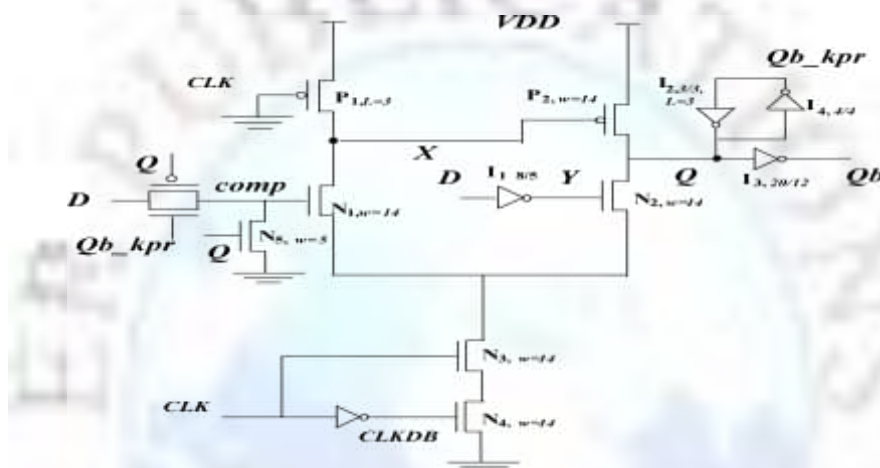


Fig. 1 Clocked-Pair Shared Flip-flop.

The pseudo NMOS transistor that is PMOS, P1, is used to charge the internal node X despite being using the two clocked pre charging transistors (P1, P2) which is used in CDMFF. By comparing CDMFF with CPSFF, a total of three clocked loads are reduced in CPSFF, such that the clock load seen by the clock driver is minimized, resulting in an efficient design. CPSFF uses four clocked loads despite of seven clocked loads which is used in CDMFF, it result in about 40% reduction in number of clocked loads. Additional to this the internal node X is connected to supply voltage V_{dd} with the help of a pseudo NMOS P1, so is not floating point is now present, and result also shows an improvement in the noise robustness of node X.

When input D stays at HIGH level then $Q=1$, here N5 is kept ON, N1 will be kept off to avoid the redundant transient activity at node X, as well as in any short circuit current. PMOS P2 is allowed to pull Q to high level when D switches to 1 value. Then second NMOS branch (N2) is in charge for pulling down the output of Q if $D = \text{LOW}$ value and $Y=1$ when the clock pulse is arrives. PMOS present in N1 should turn on NMOS N2 when $D=\text{LOW}$. Although P1 is always ON, short circuit only occurs one time when D makes a transition from LOW to HIGH, and then discharge path is disconnected after two gates delay. After all that, if at this time also D remains at HIGH, then the discharge path is already disconnected by N1; there would be no short circuit. Here the clocked-pseudo-NMOS scheme is different from the general idea of common pseudo-NMOS logic. In the previous one we use clocked transistors in the pull down branch. P1, N1, N3, and N4 should be properly scaled to guarantee a correct noise margin. CPSFF uses three less clocked loads, which by default leads to about 40% reduction in number of clocked loads. It achieves 25% less clock driving power consumption than CDMFF, which improves power efficiency.

III Power calculation using HSPICE

HSPICE is an analog circuit simulator capable of performing transient, steady state, and frequency domain analyses. Synopsys HSPICE is an optimizing analogy circuit simulator. It can be used to simulate electrical circuits in steady-

state, transient, and frequency domains. HSPICE is unequalled for fast, accurate circuit and behavioural simulation. It facilitates circuit-level analysis of performance and yield, by using Monte Carlo, worst-case, parametric sweep, and data-table sweep analyses, and employs the most reliable automatic-convergence capability. Synopsys HSPICE is compatible with most SPICE variations and has the following additional features:

- Superior convergence
- Accurate modeling, including many foundry models
- Hierarchical node naming and reference
- Circuit optimization for models and cells, with incremental or simultaneous parameter optimizations in AC, DC, and transient simulations
- Interpreted Monte Carlo and worst-case design support
- Input, output, and behavioral algebraics for cells with parameters
- Cell characterization tools to characterize standard cell libraries

The size of the circuits that HSPICE can simulate is limited only by memory. As a 32-bit application, HSPICE can address a maximum of 2Gb or 4Gb of memory, depending on the system. HSPICE stores input sweep parameters and measure output parameter, in measure output data files (design.mt0, design.sw0, and design.ac0). These files store multiple sweep data. It can use AvanWaves to plot this data; for example, to generate fanout plots of delay versus load. It can also use the slope and intercept of the loading curves to calibrate VHDL, Verilog, Lsim, TimeMill, and Synopsys models.

HSPICE operate on an input netlist file, and store results in either an output listing file or a graph data file. An input file, with the name<design>.sp, contains the following:

- Design netlist (subcircuits, macros, power supplies, and so on).
- Statement naming the library to use (optional).
- Specifies the type of analysis to run (optional).
- specifies the type of output desired (optional)

An input filename can be up to 1024 characters long. The input netlist file cannot be in a packed or compressed format. To generate input netlist and library input files, HSPICE uses either a schematic netlist or a text editor. Statements in the input netlist file can be in any order, except that the first line is a title line, and the last .Alter submodule must appear at the end of the file and before the .END statement. Area is estimated with the help of MICROWIND. All considered approaches are evaluated for the performance by using a single, low-V_{th} for all transistors. Dual V_{th} technology is applied and tested only for the sleep, dual sleep, dual stack and proposed approaches since applying high-V_{th}. For the dual V_{th} technique, high-V_{th} is used for leakage reduction transistors and low-V_{th} is used for the other transistors. Here chosen technologies are 90 Nano meter and 45 Nano meter their supply voltages are given in Table I

Chosen Technology	90 nm	45 nm
V _{dd} value	1 v	1.2 v

Table. I Chosen Technology And V_{dd} Value

The simulation results for all flip-flops were obtained in a 90nm CMOS technology at room temperature using HSPICE, the supply voltage is 1 V and again in 45 nm technology with voltage 1.2 V. In order to obtain the accurate results, we have simulated the circuits in the real environment, which dictates that the flip-flops' inputs (clock, data) are driven by fixed input buffers, and the outputs are required to drive an output load. The output waveform of CPSFF is shown below

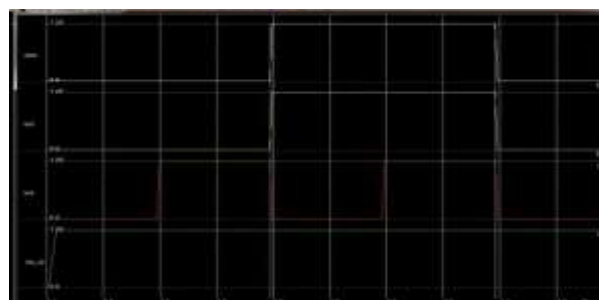


Fig 2 waveform of CPSFF

Below table shows the the comparison of the power of CPSFF flip flop in two different technology

CMOS Technology	Power (watt)
90nm	6.829E-04
45nm	8.699E-11

Table. 2 Chosen Technology And Power Value

Conclusion

The paper surveyed various clocking system and among then the clock pared shared flip flop(CPSFF) is best suited for the using as the sequential circuit in the clocking system. Along with this clocking system various low power techniques are also surveyed which help in lowering the static power in any circuit. The comparison of the power in two technologies is also tabulated above.

References

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