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Design and Analysis of Two Low Power Source Coupled Logic Structures

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Abstract: This paper presents a novel approach to design robust source coupled logic for implementing ultra low power circuits. In this paper, we proposed two different source coupled logic structures and analyzed the performance of these structures with STSCL. The first design we used DTPMOS as load device and analyses the performance of DTSCL Logic with previous source coupled logic for ultra low power operation. DTSCL circuits exhibit a better power–delay Performance compared with the STSCL Logic. It can be seen that the proposed circuit provides 56% reduction in power delay product. The second design uses basic current mirror active load device to provide required voltage swing. Current mirror source coupled logic can be used for high speed operation. The advantage of this design is that it provides 54%reduction in power delay product over conventional STSCL. The main drawback of this design is that it provides a higher power dissipation compared to other source coupled logic structures. The proposed circuit provides lower sensitivity to temperature and power supply variation, with a superior control on power dissipation [1]. Measurements of test structures simulated in 0.18 µm CMOS technology shows that the proposed DTSCL logic concept can be utilized successfully for bias currents as low as 1 pA [2]. Measurements show that existing standard cell libraries offer a good solution for ultra low power SCL circuits.

Index Terms: CMOS integrated circuits, CMOS logic circuit, DTMOS, power delay product, source-coupled logic (SCL), sub-threshold CMOS, sub-threshold SCL, ultra-low-power circuits, weak inversion.

Introduction

The increasing attention on power consumption in circuit design has motivated a significant investigation of optimum design for minimizing energy or power for a given performance constraint. Technology scaling results in a significant increase in leakage current of CMOS device**.** Various methods and techniques, such as voltage scaling, clock gating, etc. [1]–[3] have been applied successfully in the medium power, medium performance region of the design spectrum for lower power consumption. Nevertheless, in some applications where ultra-low power consumption is the primary requirement and performance is of secondary importance, a more aggressive approach is warranted. Special circuit techniques have been implemented to enable operation at very low current levels and to achieve the desired performance specifications. The demand for implementing ultra-low-power digital systems in many modern applications such as mobile systems [2],[3],[4], sensor networks [5], [6], and implanted biomedical systems [7], has increased the importance of designing logic circuits in sub-threshold regime [8].

The power dissipation is a crucial parameter in ultra-low power application. The supply voltage V_{DD} is generally reduced below the threshold voltage V_T of metal– oxide–semiconductor (MOS) devices [9]. Reducing the supply voltage or choosing high-threshold-voltage (HVT) devices results in a smaller $V_{eff} = V_{DD} - V_T$ value and, hence, less power consumption [10]. However, reducing V_{eff} results in reduction in the ratio of the ON-current of a logic gate I_{ON} to its leakage current I_{OFF}. Reduction in $\gamma = I_{ON}/I_{OFF}$ results in degradation of reliability and power efficiency of the circuit, requiring special design techniques to implement robust logic operations [9]. Sub-threshold operation (where $V_{DD}<V_T$) is currently used for some low-power applications such as watches and hearing aids. Emerging ultra-low-power applications such as distributed sensor networks are a natural fit with sub-threshold circuits. Special circuit techniques for improving robustness in deep sub-threshold have been explored [9]. In mixed mode integrated circuits the crucial parameters that affect the performance of the digital system are supply noise and substrate noise. Source coupled logic (SCL) are widely used to reduce the output voltage swing compared to CMOS logic gates for high frequency application. This paper explores performance comparison of two source coupled logic structures with previously available sub-threshold source coupled logic gates for implementing ultra-low-power digital systems. In this approach, the power consumption and maximum speed of operation can be adjusted linearly through the tail bias current of each gate over a very wide range [11], [12], thus, efficiently decoupling the decision of output voltage swing from power dissipation and delay.To enable the operation at very low trail bias current and to achieve the desired performance, we have to use a special circuit technique for implementing very low power SCL circuit. In first design, the intrinsically

limited output impedance of deep-submicron, dynamic threshold PMOS devices have been used to implement very high value load resistances for SCL topology. In second design a active load current mirror has been used to implement very high value of load resistance. Here, a more general approach with much less sensitivity to process and technology variations will be introduced [12].This paper presents two different techniques, one for implementing dynamic threshold SCL (DTSCL) gates where the bias current of each cell can be set as low as 0.1 pA and another for implementing current mirror source coupled logic gates where the bias current of each cell can be set as high as 1mA. In Section II, after a brief review of SCL circuits, the proposed techniques for implementing different SCL gates will be introduced. Section III discusses the power-delay performance of the proposed circuit configurations. Experimental results and comparison with sub-threshold source coupled logic (STSCL) circuits are presented in Section IV, followed by conclusions in Section V [2].

DIFFERENT SOURCE- COUPLED LOGIC

DTMOS Topology

In DTMOS logic, gates of transistors are tied to their substrates to achieve the same stability with direct substrate biasing without using additional control circuitry as in case of VTCMOS logic(Fig. 1)[11]. As the substrate voltage in DTMOS logic changes with the gate input voltage, the threshold voltage is dynamically changed. In the off-state, i.e., Vin=0(Vin=Vdd) for NMOS (PMOS), the characteristics of DTMOS transistor is exactly the same as regular MOS transistor. Both have the same properties, such as the same off-current, sub-threshold slope, and threshold voltage. In the on-state, however, the substrate-source voltage (vbs) for NMOS (PMOS), the characteristics of DTMOS transistor is exactly the same as regular MOS transistor. When the DTMOS is in off state then it offers higher threshold voltage which in terms reduces the leakage current of the MOS device. In the on state, the substrate-source voltage (Vbs) increases which in terms reduces threshold voltage of the DTMOS. Reduction in threshold voltage is due to the reduction in body charge which again leads to an advantage of higher carrier mobility because the reduced body charge causes a lower effective normal field. The reduced threshold, lower normal effective electric field, and higher mobility results in higher on current drive in DTMOS than that of a simple MOS transistor.

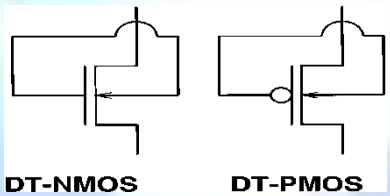


Fig.1: DT-NMOS and DT-PMOS [11].

The sub-threshold slope of DTMOS improves and approaches the ideal 60mV/decade which makes it more efficient in sub threshold logic circuits to obtain higher gain.

CURRENT MIRROR Topology

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being 'copied' can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal current amplifier. The current mirror is used to provide bias currents and active loads to circuits. There are three main specifications that characterize a current mirror. The first is the current level it produces. The second is its AC output resistance, which determines how much the output current varies with the voltage applied to the mirror. The third specification is the minimum voltage drop across the mirror necessary to make it work properly. This minimum voltage is dictated by the need to keep the output transistor of the mirror in active mode. The range of voltages where the mirror works is called the compliance range and the voltage marking the boundary between good and bad behavior is called the compliance voltage. There are also a number of secondary performance issues with mirrors, for example, temperature stability.

Basic SCL Topology

The source coupled logic (SCL) topology has been a modern approach for designing of ultra low power circuits. This topology is very suitable for very low bias current operations as it provides accurate control on power consumption of each gate, where as the power dissipation of conventional static CMOS circuits is limited by their sub-threshold leakage current. Simultaneously, the gate delay in this configuration does not depend on the supply voltage and hence, there is low sensitivity to supply voltage variations.

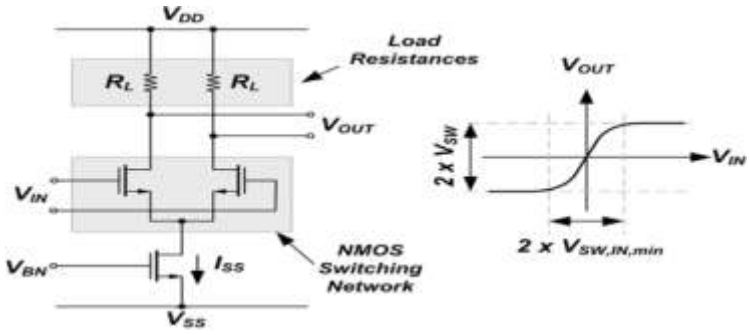


Fig.2: A conventional SCL-based inverter/buffer circuit. The switching part can be composed of a network of NMOS source-coupled pairs to implement more complex logic functions [2]. The load resistances can be implemented using PMOS devices biased in triode region

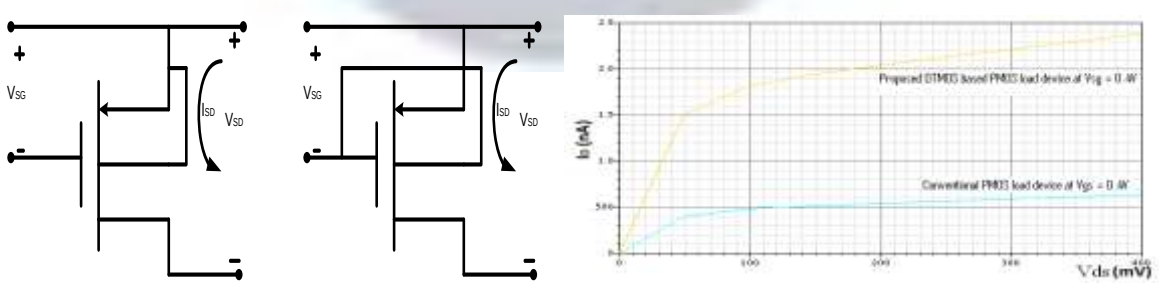
In an SCL gate, the logic operation takes place mainly in current domain. Therefore, the speed of operation can be inherently high. The voltage swing at the output node ($V_{SW}=I_{SS}\cdot R_L$) should be $V_{SW}>4n_n\cdot U_T$ (n_n is the sub-threshold slope factor of NMOS differential pair devices, and U_T is the thermal voltage).to achieve the required voltage swing at very low trail bias current the load resistance should be very high, and also occupy a small area with a very good control to adjust their resistivity with respect to their trail bias current. In first design, DTPMOS transistor can be used to provide high resistance with a relatively high voltage swing at the output, the proposed topology can operate properly as logic device. In the second design, current mirror active load is used as a load device to provide higher resistance with a relatively high voltage swing.In SCL topology the main leakage currents are due to the p-n junctions of the MOS devices, whereas in CMOS logic circuits the sub-threshold channel leakage current is the dominant leakage component,. The speed of operation in an SCL gate is mainly limited by the time constant at the output node which is

$$T_{SCL} = R_L \cdot C_L = V_{SW} \cdot C_L/I_{SS}. \qquad (1)$$

Based on this, the propagation delay is inversely proportional to the tail bias current. Meanwhile, the circuit power–delay product (PDP) is independent of I_{SS} [12], [13], [14].

Load Device Concept

To maintain the required voltage swing at very low trail bias current it is necessary to increase the load resistance in inverse proportion to the reducing trail bias current. In sub-threshold region, the trail bias current would be in the order of few pA or even less. Therefore, to obtain a required output voltage swing, the load resistance should be of the order of few GΩ. Meanwhile, this resistance should be controlled very accurately based on the value of trail bias current Iss. Hence, a well controlled high resistivity load device with a very small area is required. For this range of resistivity, conventional PMOS devices biased in triode region cannot be utilized since the required channel length of the transistor would be impractically large. Fig. 3(b) shows the proposed load device, where the gate of the PMOS device is connected to its bulk. In this way, the load device provides accurate control on the resistance, which, associated with the trans-conductance of the differential pair will provide a controlled, limited gain and amplitude with relatively small size PMOS load device.



(a) (b) (c)

Fig.3. (a) Conventional PMOS load device, (b) DT-PMOS load device, (c) I–V characteristics of the conventional PMOS load in comparison to the proposed DT-PMOS device.

In the proposed load device the gate and substrate of PMOS load device are shorted. When $V_{SG} = V_{SD}$ then it will behave as conventional PMOS load device as we vary the gate voltage V_{SG} the voltage across the substrate terminal also varies as a result the threshold voltage of the device changes and also the resistance of the PMOS load device varies. In this way the proposed load device will be used as a controlled resistance.

The basic current mirror can also be implemented using MOSFET transistors, as shown in Figure. 4. Transistor M_1 is operating in the saturation or active mode, and so is M_2. In this setup, the output current I_{OUT} is directly related to I_{REF}. The drain current of a MOSFET I_D is a function of both the gate-source voltage and the drain-to-gate voltage of the MOSFET given by $I_D = f(V_{GS}, V_{DG})$, a relationship derived from the functionality of the MOSFET device. In the case of transistor M_1 of the mirror, $I_D = I_{REF}$. Reference current I_{REF} is a known current, and can be provided by a resistor as shown, or by a "threshold-referenced" or "self-biased" current source to ensure that it is constant, independent of voltage supply variations.

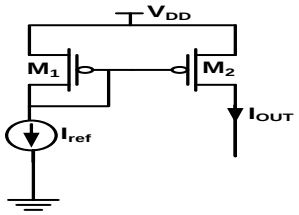


Figure. 4: The basic current mirror structure.

Using $V_{DG}=0$ for transistor M_1, the drain current in M_1 is $I_D = f(V_{GS},V_{DG}=0)$, so we find: $f(V_{GS}, 0) = I_{REF}$, implicitly determining the value of V_{GS}. Thus I_{REF} sets the value of V_{GS}. The circuit in the diagram forces the same V_{GS} to apply to transistor M_2. If M_2 also is biased with zero V_{DG} and provided transistors M_1 and M_2 have good matching of their properties, such as channel length, width, threshold voltage etc., the relationship $I_{OUT} = f(V_{GS},V_{DG}=0)$ applies, thus setting $I_{OUT} = I_{REF}$; that is, the output current is the same as the reference current when $V_{DG}=0$ for the output transistor, and both transistors are matched. The drain-to-source voltage can be expressed as $V_{DS}=V_{DG} +V_{GS}$. With this substitution, the Shichman-Hodges model provides an approximate form for function $f(V_{GS},V_{DG})$

$$I_d = f\ (V_{GS}, V_{DG}) = \tfrac{1}{2}K_p\left(\tfrac{W}{L}\right)(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$
$$= \tfrac{1}{2}K_p\left(\tfrac{W}{L}\right)(V_{GS} - V_{th})^2\,(1 + \lambda(V_{DG} + V_{GS}))$$

Where, K_p is a technology related constant associated with the transistor, W/L is the width to length ratio of the transistor, V_{GS} is the gate-source voltage, V_{th} is the threshold voltage, λ is the channel length modulation constant, and V_{DS} is the drain source voltage.Because of channel-length modulation, the mirror has a finite output (or Norton) resistance given by the r_o of the output transistor, namely

$$R_N = r_o = \frac{1/\lambda + V_{DS}}{I_D},$$

Where λ = channel-length modulation parameter and V_{DS} = drain-to-source bias.

DTSCL Gates

The proposed DTPMOS load device can be utilized to implement an SCL gate biased in sub-threshold regime. Fig. 5 shows the basic structure of the proposed DTSCL gate. A simplified circuit diagram of the replica bias circuit used to control the output voltage swing is also shown. In this schematic, all devices operate in sub-threshold regime and the tail bias current can be reduced until it becomes comparable in magnitude to the leakage currents that exist in the circuit. Fig. 6(a) illustrates the DC transfer characteristics of an DTSCL gate. The stage gain of DTSCL gate is as shown in fig .6(b). The measured stage gain of DTSCL gate is approximately 42. The measured input–output transfer characteristics of a DTSCL buffer stage at different trail bias current are shown in Fig. 6(c).As all the devices are operating in sub-threshold regime hence the transfer characteristic of the circuit is independent of the trail bias current.

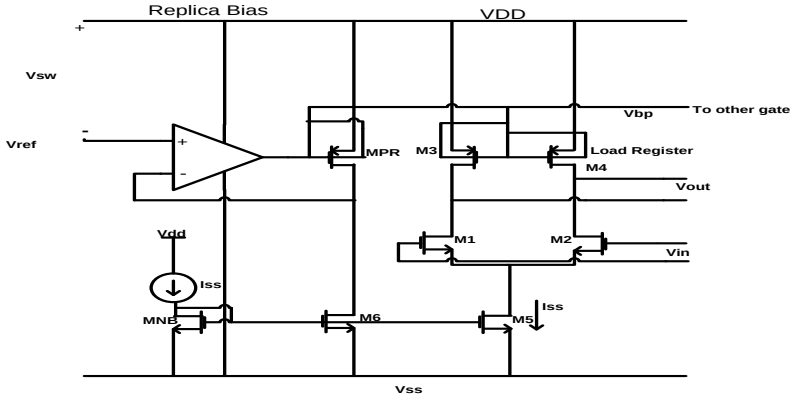
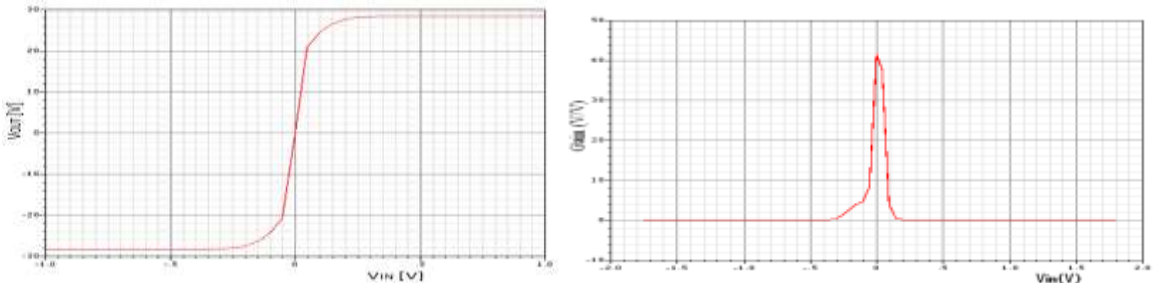
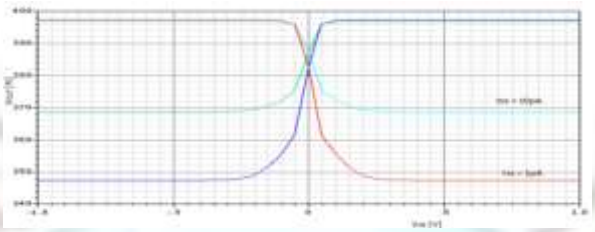


Fig.5. DTSCL gate and the replica bias circuit used to control the output voltage swing.

In this plot, the deviation from the ideal DC characteristics is mainly due to the leakage currents in the test circuit coming from electrostatic discharge (ESD) protection circuitry. To measure the DC characteristics, output voltage swing has been adjusted manually.



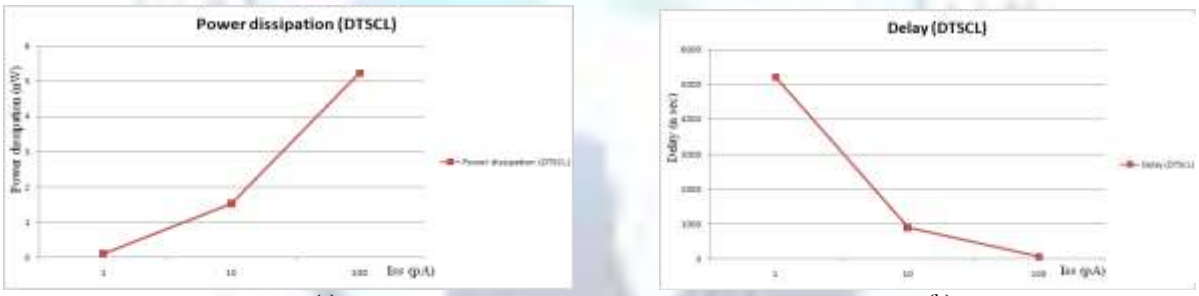
(a) (b)



(c)

Fig.6. (a) Simulated DC transfer characteristics of a DTSCL gate biased at I_{SS} = 1 pA. (b) DC gain of a DTSCL gate biased at I_{SS} = 1 pA. (c)Measured transfer characteristics of a DTSCL buffer stage for different bias currents (I_{SS} = 1 pA, and 10 pA).

The variation in power dissipation and gate delay of a DTSCL gate is as shown in fig. and fig. simultaneously. It is seen that the stabilized output of is achieved at trail bias current ISS = 1 pA. At this trail bias current, DTSCL provides lowest power delay product of the order of 569.71x10^{-18} W-Sec.



(a) (b)

Fig.7.(a) variation in power dissipation with trail bias current.(b)variation in delay with trail bias current.

Current Mirror SCL Gates

The proposed current mirror active load device can be utilized to implement an SCL gate biased in sub-threshold regime. Fig. 8 shows the basic structure of the proposed Current Mirror SCL gate.

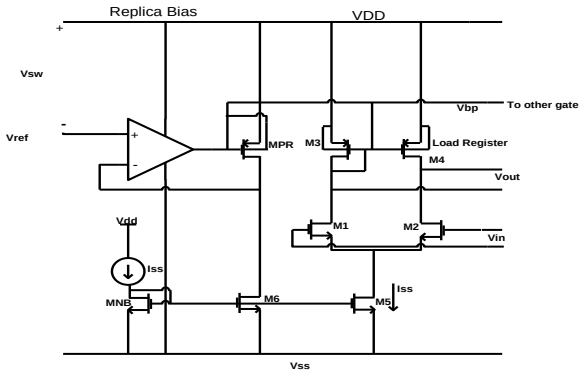
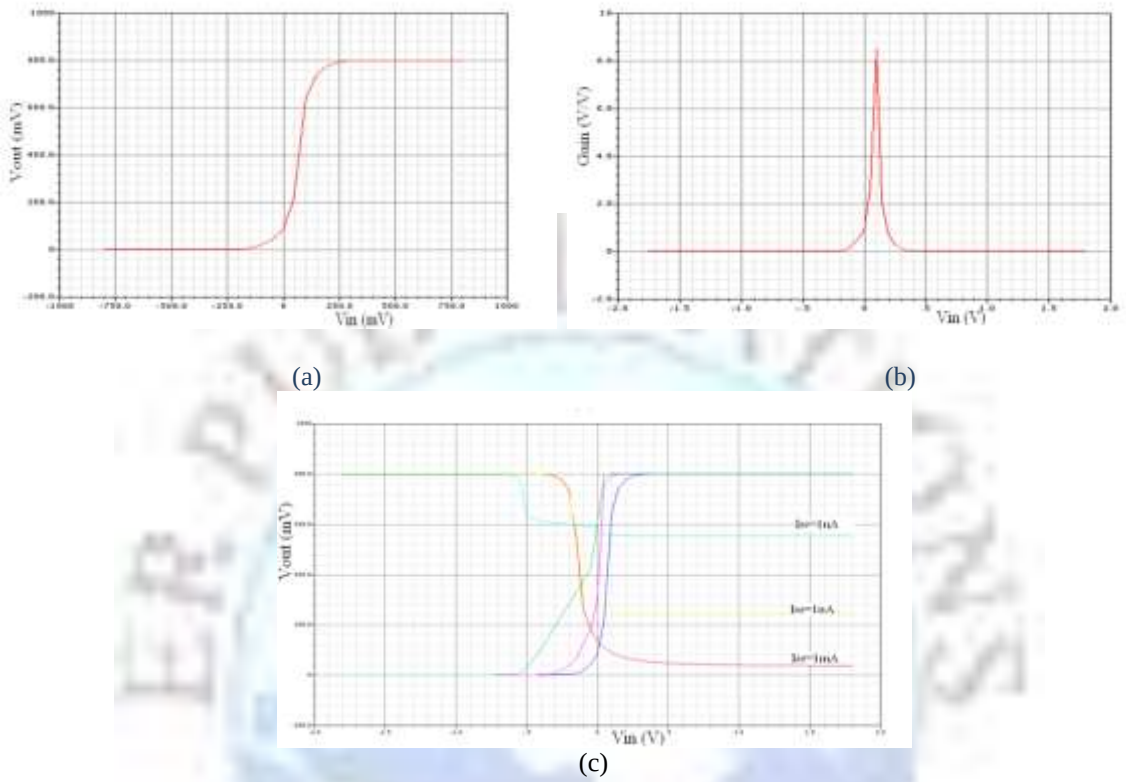


Fig.8. Current Mirror SCL gate and the replica bias circuit used to control the output voltage swing.

In this schematic, all devices operate in sub-threshold regime and the tail bias current can be reduced until it becomes comparable in magnitude to the leakage currents that exist in the circuit. Fig. 9(a) illustrates the DC transfer characteristics of a Current Mirror SCL gate. The stage gain of Current Mirror SCL gate is as shown in fig .9(b). The measured stage gain of Current Mirror SCL gate is approximately 8.2. The measured input–output transfer characteristics of a Current Mirror SCL buffer stage at different trail bias current are shown in Fig. 9(c).As all the devices are operating in sub-threshold regime hence the transfer characteristic of the circuit is independent of the trail bias current. In this plot, the deviation from the ideal DC characteristics is mainly due to the leakage currents in the test circuit coming from electrostatic discharge (ESD) protection circuitry. To measure the DC characteristics, output voltage swing has been adjusted manually.

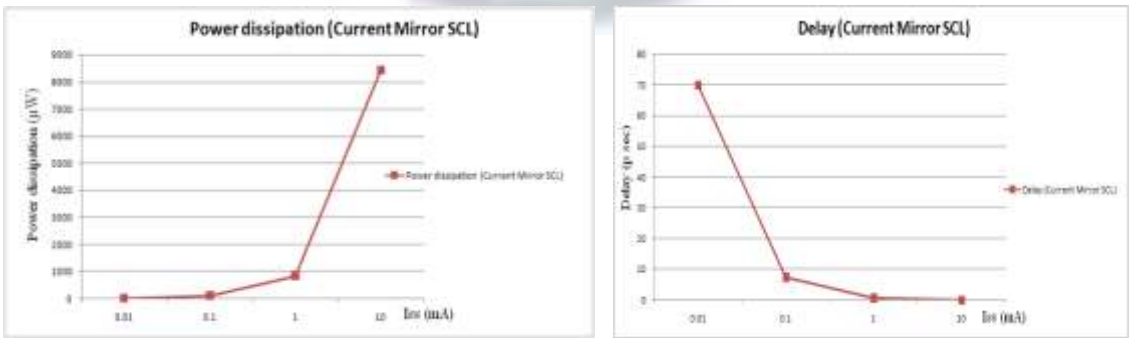


(a) (b)

(c)

Fig.9. (a) Simulated DC transfer characteristics of a Current Mirror SCL gate biased at I_{SS} = 1 mA. (b) DC gain of a Current Mirror SCL gate biased at I_{SS} = 1 mA. (c)Measured transfer characteristics of a Current Mirror SCL buffer stage for different bias currents (I_{SS} = 1nA, 1µA and 1mA).

The variation in power dissipation and gate delay of a Current Mirror SCL gate is as shown in fig. and fig. simultaneously. It is seen that the stabilized output of is achieved at trail bias current I_{SS} = 1 mA. At this trail bias current, Current Mirror SCL provides lowest power delay product of the order of 592.238x10^{-18} W-Sec.



(a) (b)

Fig.10.(a) variation in power dissipation with trail bias current. (b) Variation in delay with trail bias current.

Voltage Swing Control

To achieve the required voltage swing at the output, a controlling circuit is used. Fig. 11 shows a simplified schematic of replica bias circuit to control the output voltage swing. The Replica bias circuit consists of a high performance current mirror circuit that can maintain a constant current I_{SS} at the output to provide accurate control on the output

voltage swing. The replica bias circuit should be well matched to the SCL gates to have very low deviation in operating point. Meanwhile, amplifier should provide enough gain with a very low offset to have the desired accuracy. In this work, a folded-cascode amplifier has been used to provide a large swing at the output node and to be able to test the SCL gates in a very wide range of bias current values. Any mismatch in the bias current or devices of the SCL gates and RB circuit will result in variation of the desired output voltage swing and it can be shown that the sensitivity of this circuit to the mismatches is

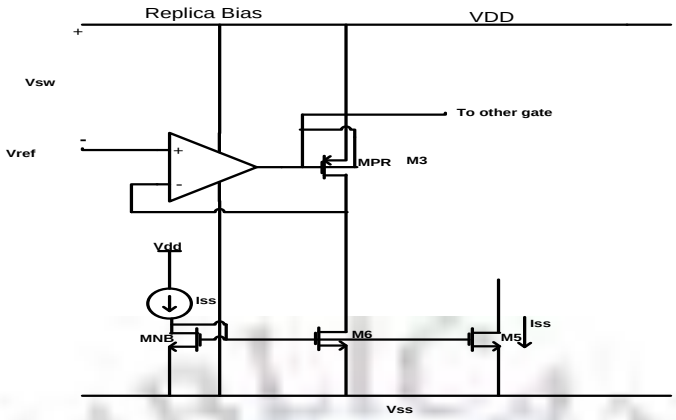


Fig.11 Replica bias circuit to control output voltage swing.

PERFORMANCE ANALYSIS AND OBSERVATION

A. Power–Speed Tradeoff in SCL Circuits

In contrast to the CMOS gates, where there is no static power consumption (neglecting the leakage current), each SCL gate draws a constant bias current of I_{SS} from a supply source (Fig. 2). Therefore, the power consumption of each SCL gate can be calculated by

$$P_{diss,SCL\ 1}=V_{DD}I_{SS}. \quad (1)$$

Meanwhile , the time constant at the output node of each SCL gate, i.e.

$$\tau=R_L\cdot C_L\approx(V_{SW}/I_{SS})\cdot C_L \quad (2)$$

is the main speed-limiting factor in this topology (C_L is the total output loading capacitance). Based on (2), one can choose the proper I_{SS} value to operate at the desired frequency. This circuit exhibits a very low sensitivity to the process variations because the power consumption and delay of each gate only depend on I_{SS}, which can very precisely be controlled. Meanwhile, it is not necessary to use special process options to have low threshold voltage devices, as frequently used for static CMOS [1], [2], [8].

Therefore, it is necessary to use the DTSCL circuits at their maximum activity rate to achieve the maximum achievable efficiency. It is also important to note that the gate delay does not depend on the supply voltage, whereas it linearly varies with the tail bias current. This property can be exploited for applications in which the supply can vary during the operation. Based on (1) and (2), the power–delay product (PDP) of each gate can be approximately calculated by

$$PDP_{DTSCL,1}=\ln 2\times V_{DD}V_{SW}C_L \quad (3)$$

Observation 1: The delay of a logic block can be controlled without influencing PDP as the delay of DTSCL gate depends on trail bias current (I_{SS}), but not on supply voltage V_{DD}.

Observation 2: To reduce the power to frequency ratio, α should be kept as large as possible. This observation does not contradict with similar results for conventional CMOS

CONCLUSION

In this paper, an analytical approach for studying and comparing the performance of ultra low power STSCL, DTSCL, and Current Mirror SCL has been presented. While there is a tight tradeoff among the power consumption, speed of operation , and supply voltage in design of CMOS digital circuits, the SCL topology provide a more flexible deign option for ultra low power applications. In this paper, two new source coupled logic design has been discussed. The first design uses a high resistance DT-PMOS load device to provide the required voltage swing at the output. The measurement result shows that the DTSCL topology provides 56% reduction in PDP compared to STSCL, using 0.18µm CMOS technology. The second design uses basic current mirror load device to provide required voltage swing at the output. This design can be used for high speed operation but this design provides higher power dissipation. Hence this design can be used for high speed operation on the cost of power dissipation. The measurement result shows that the Current Mirror SCL provides 54% reduction in PDP compared to STSCL, using 0.18µm CMOS technology. The trail bias current of each gate can be reduced to less than 0.1pA, while the power delay product of the gate remains less

than 1 FJ. The bias current of a SCL gate can be scaled over several decades, which makes this topology very suitable for ultra low power applications. The main advantage of this topology is that there is no effect of process and temperature variation and it can operate in a wide range of frequency.

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