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# Design and Power Analysis of Sequential Circuits using Adiabatic Technique

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**ABSTRACT: One of the biggest challenges of our times is to limit the power consumed in electronic devices which will lead to longer battery life while maintaining high performance. Several different design methodologies are being probes with this end in mind. In this paper conventional CMOS and adiabatic reduction technique for D, T, SR and JK is compared and their static and average power is computed. All the circuits are simulated with and without adiabatic logic, static power consumed for D, T, SR and JK flip flops are reduced up to 4.75%, 5.27%, 18.85%, 7.08% respectively and the average power consumed are reduced up to 5.82%, 19.31%, 9.83%, 7.38% respectively. The circuits are simulated at transistor level using Cadence Virtuoso Tool at 180 nm process technology at VDD=1.8V and T=27$^0$C.**

**Keywords: Adiabatic circuits, D Flip Flop, JK Flip Flop, Low-Power, Sequential circuits, T Flip Flop, SR Flip Flop.**

## INTRODUCTION

Power reduction is one of the major concern as lower technologies have increased the number of transistors on a chip leading to problems like IC packaging and reliability [1]. Longer battery life in high performance devices is the demand of the day. Methods for power reduction based on the application of adiabatic techniques to CMOS circuits have recently come under renewed investigation. In Adiabatic logic, $V_{DD}$ is replaced with a periodic ramp signal or an AC power supply. The main idea in an adiabatic charging is that transitions are considered to be sufficiently slow so that all the nodes are charged or discharged at a constant current. In this way power dissipation is minimized by decreasing the peak current flow through the transistors. [2,3,4].

## A REVIEW OF RELATED WORK

### A. Fundamental Logics based on Two Phase Clocked Adiabatic CMOS Logic

In this paper, some of the fundamental logic gates consisting of two phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. The simulations are done using SPICE tool at 180nm using 1.8 Voltage supply.

According to the simulation results at 10 to 100 MHz frequencies the 2PASCL inverter logic is able to control 97% of energy dissipation in comparison with a static CMOS logic [5].

From the simulation results we can conclude that for low power digital device applications operated at low frequencies, 2PASCL technology can be used in efficient way as when compared with other proposed adiabatic logic inverters the power dissipation of the proposed 2PASCL inverter is lowest.

### B. Adiabatic Logic: Energy Efficient Technique For Vlsi Applications

This paper proposed an energy efficient technique with two-phase clocked adiabatic logic on NAND, NOR, and Adiabatic logic Inverter circuit. The simulations have been carried out in SPICE at 180nm technology. Further NAND and NOR gates have been implemented by this technique and hence compared with the standard CMOS, Positive Feedback Adiabatic Logic (PFAL) and Two-Phase Adiabatic Static Clocked Logic (2PASCL) logic. The simulation results shows the comparison of significant power saving to the extent of 70% in case of proposed technique as compared to CMOS logic within 10 to 150MHz transition frequency range.[6]

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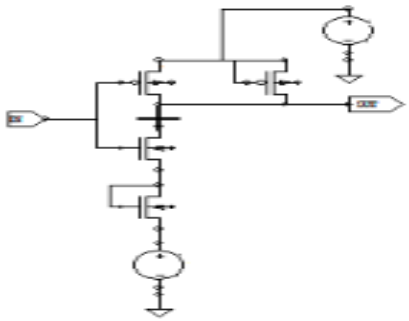

**Figure I: 2 PASCL Logic Circuit [7]**

## SIMULATION AND RESULTS

In this section comparison of conventional sequential circuits and adiabatic sequential circuits on the basis of average power dissipation and static power dissipation has been carried out. In general or conventional CMOS circuit designing DC power supply is used whereas in adiabatic logic AC power supply is used rather than DC power supply.

The following parameters are taken in to account while designing.

**TABLE I Width (W) and Length (L) for NMOS and PMOS**

| Technology | 180nm |
|---|---|
| W(NMOS) | 2µm |
| L(NMOS) | 18µm |
| W(PMOS) | 2 µm |
| L(PMOS) | 18 µm |

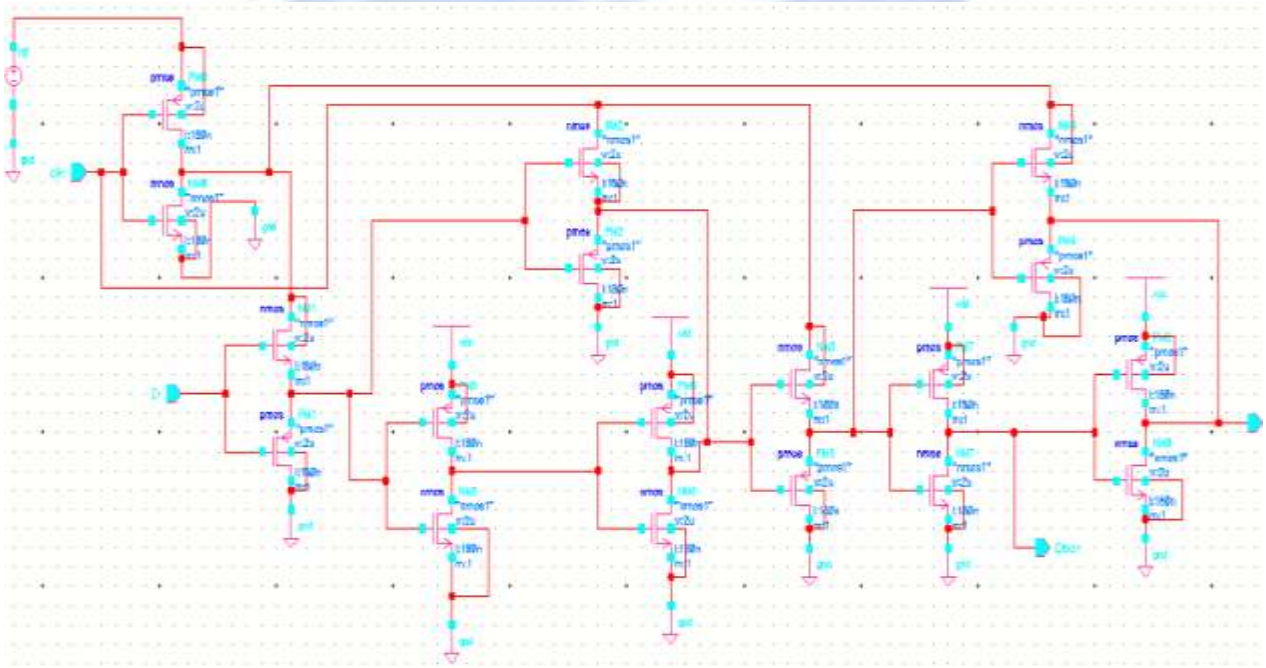

**Figure II: Schematic of D Flip Flop**

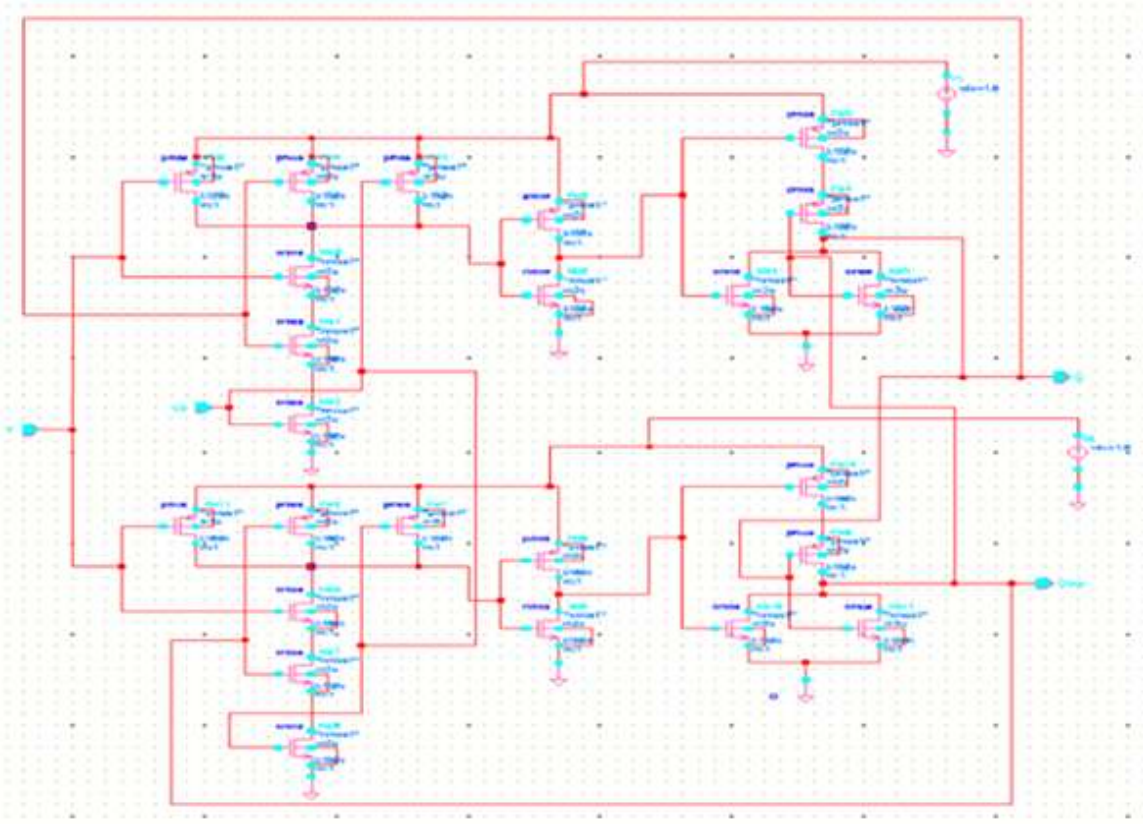

**Figure III Schematic of T Flip Flop**

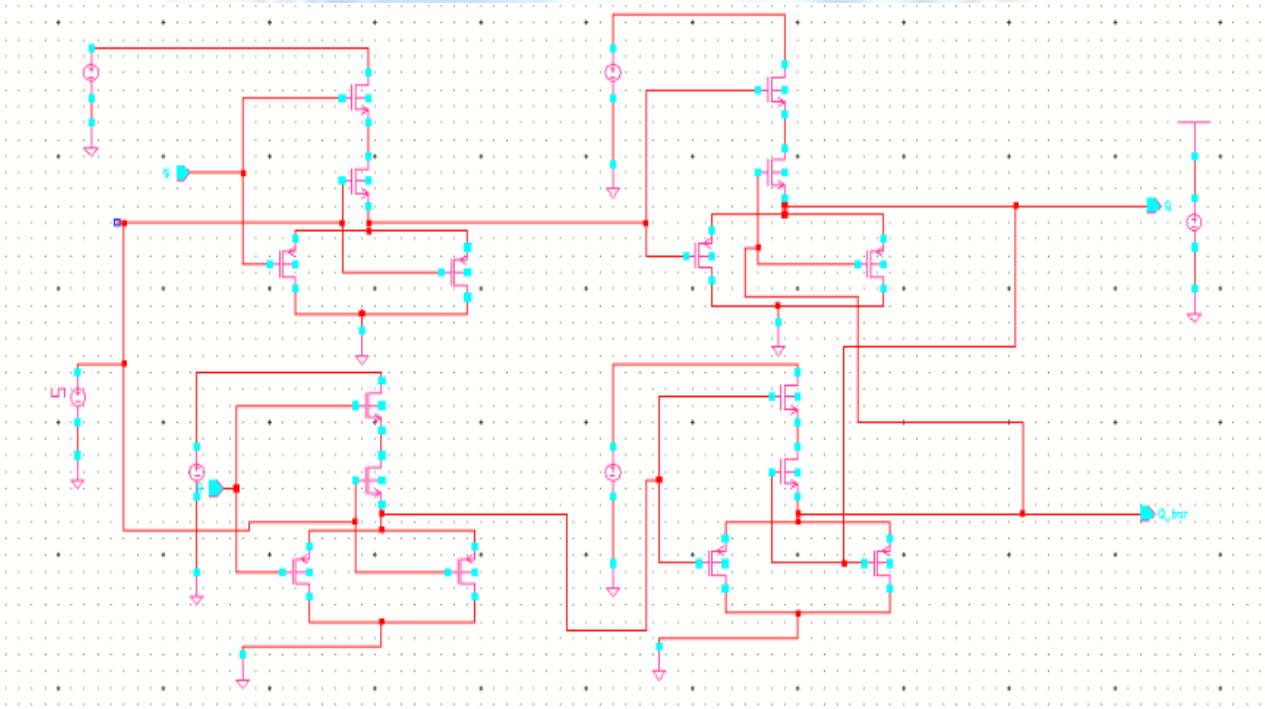


**Figure IV Schematic of SR Flip Flop**

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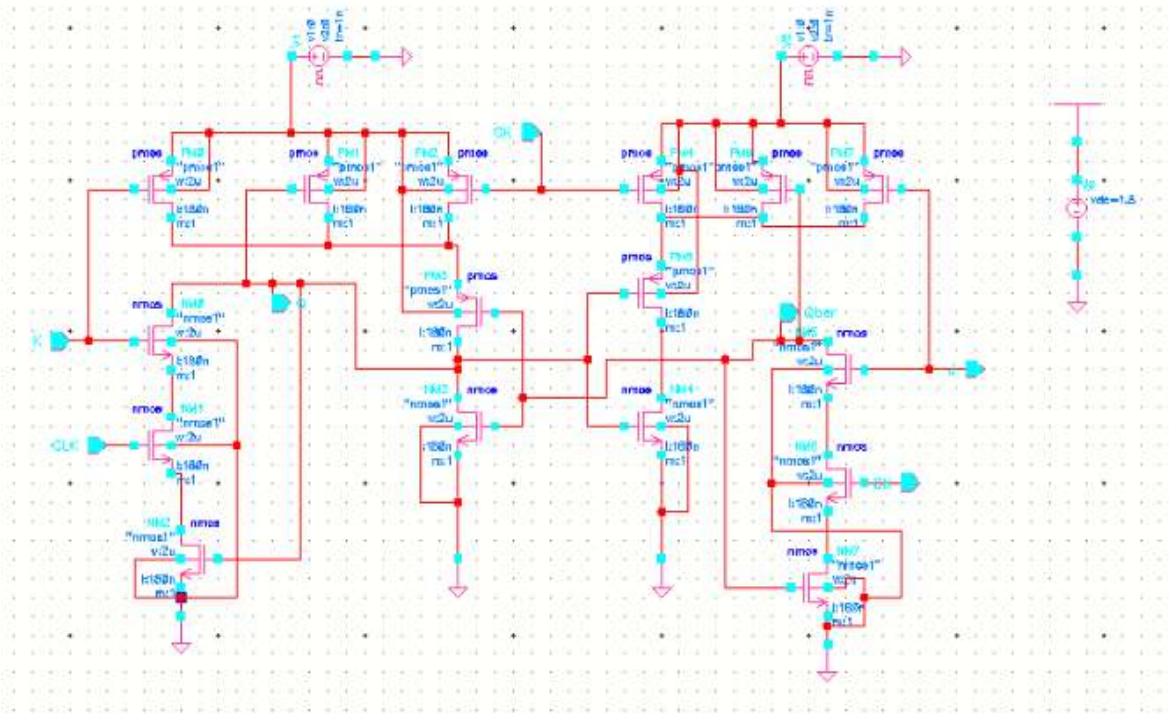


**Figure V Schematic of JK Flip Flop**

Tables and Figures showed below shows the comparison of average and static power dissipation for conventional and adiabatic sequential circuits.

**Table II shows the comparison of average power dissipation of conventional and adiabatic sequential circuits**

| SCHEMATIC | POWER CONSUMPTION (µW) | ADIABATIC POWER CONSUMPTION (µW) |
|---|---|---|
| | AVERAGE | AVERAGE |
| D FLIP FLOP | 64.88 | 61.31 |
| T FLIP FLOP | 76.4 | 64.03 |
| SR FLIP FLOP | 47.24 | 43.01 |
| JK FLIP FLOP | 55.09 | 51.3 |

**Table III show the comparison of static power dissipation of conventional and adiabatic sequential circuits**

| SCHEMATIC | POWER CONSUMPTION (µW) | ADIABATIC POWER CONSUMPTION (µW) |
|---|---|---|
| | STATIC | STATIC |
| D FLIP FLOP | 42.11 | 40.2 |
| T FLIP FLOP | 43.5 | 41.32 |
| SR FLIP FLOP | 34.74 | 29.23 |
| JK FLIP FLOP | 62.12 | 58.01 |

**Figure VI show the comparison of average power consumption of conventional and adiabatic sequential circuits**

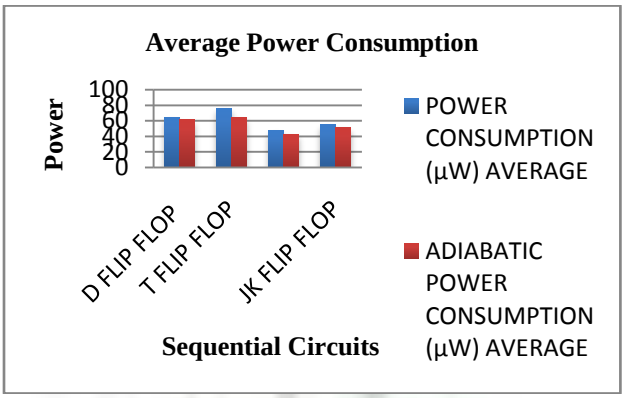



**Figure VII show the comparison of static power consumption of conventional and adiabatic Sequential circuits**

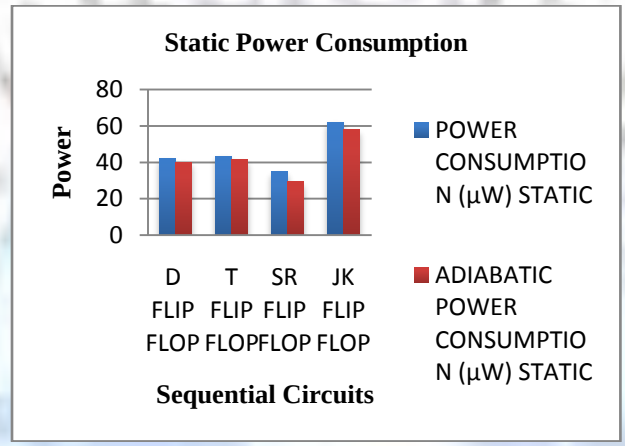
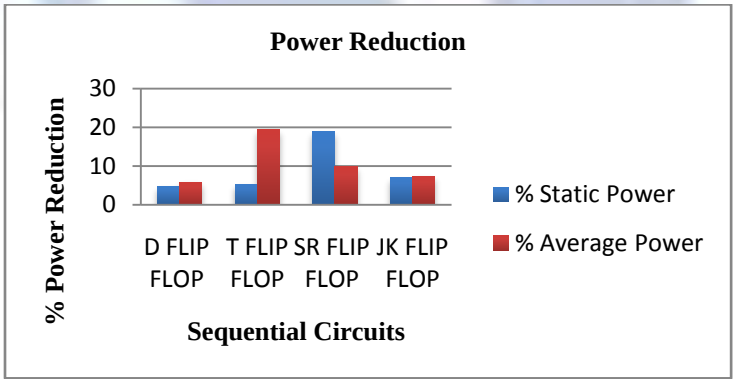



**Figure VIII Shows the %age of Static and Average Power Reduction of Different Sequential Circuits**




## Conclusions

In this work adiabatic technique is used for reduction of average power dissipation with no performance degradation. Simulation of different Sequential circuits (D, T, SR, and JK) has been done for 180nm CMOS technology on Cadence Virtuoso Tool at 1.8V supply voltage. By using this technique the static power consumed for D, T, SR, JK and 6T SRAM flip flops are reduced up to 4.75%, 5.27%, 18.85%, 7.08% respectively and the average power consumed are reduced up to 5.82%, 19.31%, 9.83%, 7.38% respectively. Simulation results shows that the T flip-flop circuit has the maximum %age of power saving. This reduction technique can be used in high performance low power circuits such as memory designing and various high end processors.

## About The Author

**Pooja Chaudhary,** completed her B.Tech in Electronics and Communication Engineering from Amity University, Noida in 2012. She is now pursuing her Master of Technology (M. Tech.) in VLSI Design at ITM University, Gurgaon (Haryana) India. Her interest includes Digital Design, VLSI Testing and Verification.

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