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Signal Integrity Analysis of High Speed Devices

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Abstract: The signal integrity analysis of the PCB signal has already seemed to be more important due to the use of high speed clock and High speed signals. This Paper Presents Signal Integrity Analysis of "High Speed Devices with Data Rate of 2.5GT/s" The comparative result shows that by proper stackup, control impedance technique, reducing dielectric thickness and proper terminations. Signal Integrity can be improved. And the Eye Diagram (eye pattern) is used to analyse the Quality and timing of High speed serial data.

Keywords: Signal Integrity, Stack up, Crosstalk, EMI/C, Eye Pattern.

I. INTRODUCTION

High-speed data rates are now common place in the world of telecommunications, computing and data networking. Data rates in high-speed digital systems are currently well into the GB/s range, and increasing rapidly. In order to meet the challenges at these data rates, design methodologies and models for developing signal link paths from the silicon transmitter, across packages, printed circuit boards, connectors, and backplanes are required. High-speed design requires not only traditional physical rules, but also true electrical rules such as delay, impedance, and phase matching. Speed, increasing power requirements, and the density of modern board designs have created major areas of concern.

Modern, volume-manufactured digital designs require control of timings down to the Pico-second range This level of timing must not only be maintained at the silicon level, but also at the physically much larger level of the system board, such as a computer motherboard. In today's world, the demand for ultra-high-speed PCB design is on the rise. These systems operate at high frequencies at which conductors no longer behave as simple wires, but instead exhibit high frequency effects and behave as transmission lines that are used to transmit or receive electrical signals to or from neighboring components. If these transmission lines are not handled properly, they can unintentionally ruin system timing. Non-intended and non-ideal characteristics such as transmission-line propagation delay, attenuation, finite impedance of the conductors, metal planes and power-supply structures, unintended current-paths, crosstalk, emission and immunity are some of the factors that must be considered during design. These characteristics are not included in the schematics, yet they play a significant role in the circuit performance. If not seriously considered they will lead to problems with signal-integrity (SI) and electromagnetic compatibility (EMC).

II. SIGNAL INTEGRITY ANALYSIS

The basic idea in digital design is to communicate information with signals representing 1s or 0s. Typically this involves sending and receiving a series of trapezoidal shaped voltage signals such as shown in the figure below in which a high voltage is 1 and a low voltage is 0. The conductive paths carrying the digital signals are known as interconnects. The interconnect includes the entire electrical pathway from the chip sending a signal to the chip receiving the signal.

Fig 1 Digital Waveform and two high speed devices with stack up

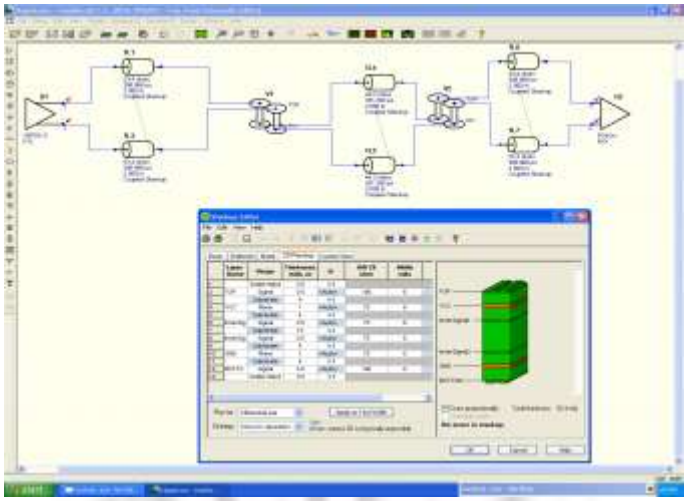

Fig 2: Stackup

A group of interconnects is referred to as a bus. The region of voltage where a digital receiver distinguishes between a high and a low voltage is known as the threshold region. Within this region, the receiver will either switch high or switch low. On the silicon, the actual switching voltages vary with temperature, supply voltage, silicon process, and other variables.

Every conductor has a capacitance, inductance, and frequency-dependent resistance. At a high enough frequency, none of these things is negligible. Thus a wire is no longer a wire but a distributed parasitic element that will have delay and a transient impedance profile that can cause distortions and glitches to manifest themselves on the waveform propagating from the driving chip to the receiving chip. The wire is now an element that is coupled to everything around it, including power and ground structures and other traces. The signal is not contained entirely in the conductor itself but is a combination of all the electric and magnetic fields around the conductor.

In today's high speed digital system it is necessary to treat the printed circuit board traces as transmission lines. It is no longer possible to model interconnects as lumped capacitors or simple delay lines as could be done on slower design.

The characteristic impedance or surge impedance of a uniform transmission line, usually written Z_0, is the ratio of the amplitudes of a single pair of voltage and current waves propagating along the line in the absence of reflections. The SI unit of characteristic impedance is the ohm. The characteristic impedance of a lossless transmission line is purely real, that is, there is no imaginary component
($Z_0 = | Z_0 | + j0$).

Characteristic impedance is of prime importance for good transmission. Maximum power transfer occurs when the source has the same impedance as the load. Thus for sending signals over a line, the transmitting equipment must have the same characteristic impedance as the line to get the maximum signal into the line. At the other end of the line, the receiving equipment must also have the same impedance as the line to be able to get the maximum signal out of the line. Perhaps the most important and most common electrical issue that keeps coming up in high speed design is controlled impedance boards and the characteristic impedance of the traces. Yet,
The ratio of voltage applied to the current is called the input impedance; the input impedance of the infinite line is called the characteristic impedance.

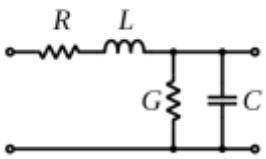

Fig 3: Schematic for an elemental length of transmission line

The general expression for the characteristic impedance of a transmission line is:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (1)$$

Where,

R is the resistance per unit length,
L is the inductance per unit length,
G is the conductance of the dielectric per unit length,
C is the capacitance per unit length,
j is the imaginary unit, and
ω is the angular frequency.

For CMOS and TTL this will be in the region of 80 to 110 ohms.

Where impedances do not match, some of the signal is reflected back towards the source. In many cases this reflected signal causes problems and is therefore undesirable. For optimal signal quality, primarily, keep the characteristic impedance of the line constant.

A. Crosstalk Analysis

The signals on one interconnect (aggressor) will affect and be affected by the signals on another (Victim). Furthermore, at high frequencies, complex interactions occur between the different parts of the same interconnect, such as the packages, connectors, vias, and bends. All these high-speed effects tend to produce strange, distorted waveforms. These things also determine how much energy the system will radiate into space, which will lead to determining whether the system complies with governmental emission requirements. One of the most difficult aspects of high-speed design is the fact that there are a large number of co-dependent variables that affect the outcome of a digital design. Some of the variables are controllable and some force the designer to live with the random variation. There are 2 kinds of crosstalk discussed. They are:

Forward Crosstalk: The crosstalk that appearing on the victim line at the receiver end due the aggressor line. It is a function of the difference between capacitive crosstalk and mutual inductance crosstalk.

Backward Crosstalk: The crosstalk appearing on the victim line at the driver end due the aggressor line. It is a function of the sum of the capacitive and mutual inductance crosstalk currents.

The comparative result shown in figure 5 and 6 implies that by using proper stackup, control impedance technique, reducing dielectric thickness and proper terminations crosstalk issues can be minimized.

B. EMI/C Analysis

Electromagnetic interference (EMI) is any electromagnetic disturbance that degrades or limits the performance of the considered electronic system. The system being considered or its environment can induce it. Electromagnetic interference (EMI) is directly proportional to the change in current or voltage with respect to time. EMI is also directly proportional to the series inductance of the circuit.

Every PCB generates EMI. The ICs are the sources of the electromagnetic interference (EMI), and the cables or metal framing act as radiating antennas. In high-speed digital circuits, the clock circuitry is usually the biggest generator of wide-band noise.

Electromagnetic compatibility (EMC) is the property of an electronic device to coexist peacefully with its electronic neighbors. This means that it must not radiate excessively into its environment and, if placed into a noisy electromagnetic environment, it must not be too sensitive (susceptible).

EMC: It states that "Ability of a system or device or an equipment to function satisfactorily in its electromagnetic environment without introducing electromagnetic disturbances in that environment".

Causes for EMI in PCB:

- Poor signal integrity handling
- Improper layout design and build
- Long current return paths
- Poor layer stack organization
- Grounding issues

The comparative result showed in the figure 7 and 8 shows that by using appropriate steps EMI issues are overcome.

C. Eye diagram Analysis

High speed serial data transfer quality analysis using eye diagram. This is carried out to check the Quality and Timing of the signal. To perform eye diagram analysis; the bits to be transmitted are overlapped on one another that take the shape of an Eye. Pseudo random bit sequence can be 7, 9, 11, 15, 21 bits. The eye is characterized by its height and width, together called as eye opening.

As trace length increases, delay increases, this results in pulse spreading and decreases eye width. This results in inter-symbol interference (ISI). If distortion or material loss occurs then eye height decreases.

The result showed in figure 9 shows the eye diagram analysis and the eye mask is within the eye opening.

III. RESULT

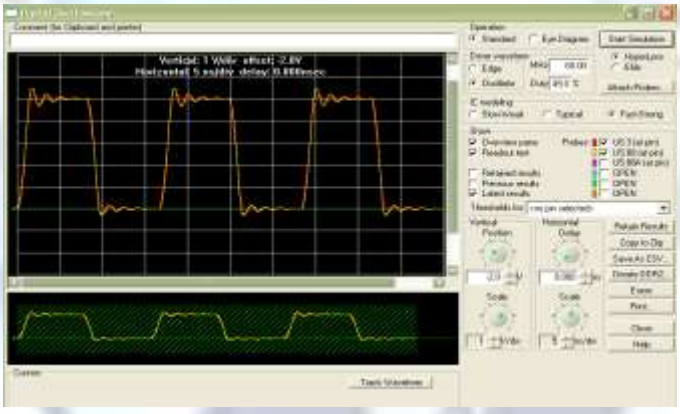

Fig 4: Simulation results without termination

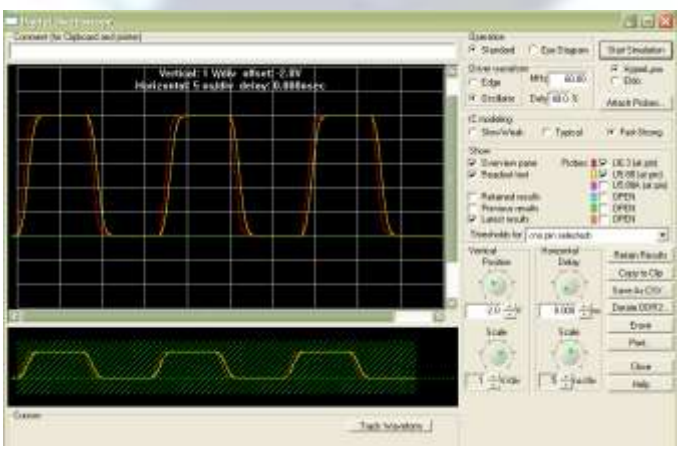

Fig 5: Simulation results with termination

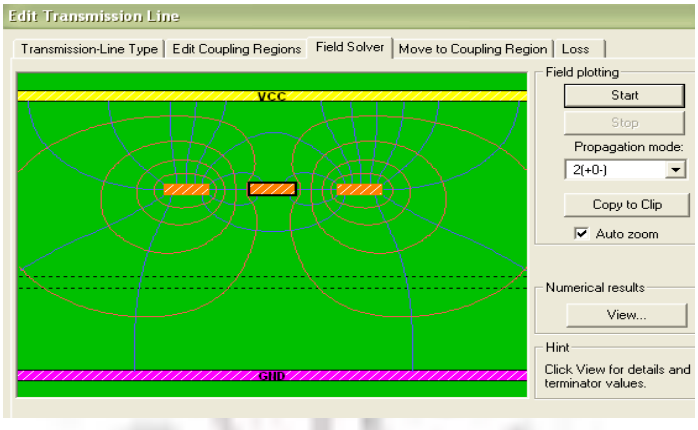

Fig 6: Crosstalk due to less spacing between traces

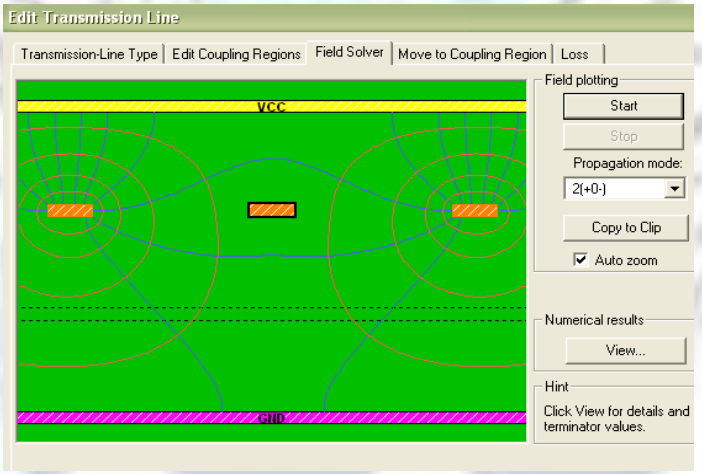

Fig 7: Crosstalk reduced, due to increase in spacing

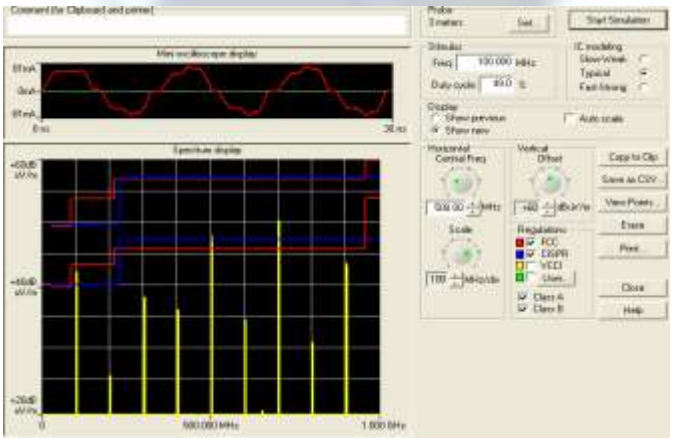

Fig 8: Simulation results without termination

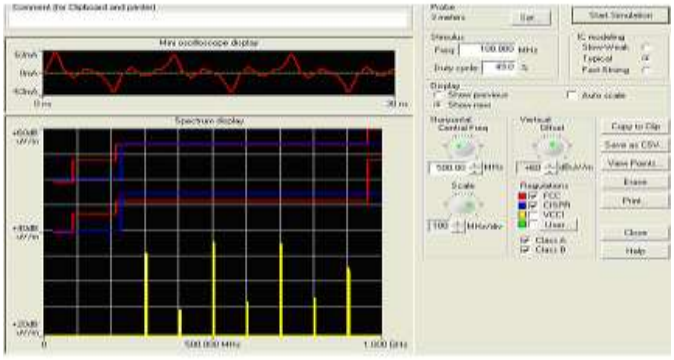

Fig 9: Simulation results with termination

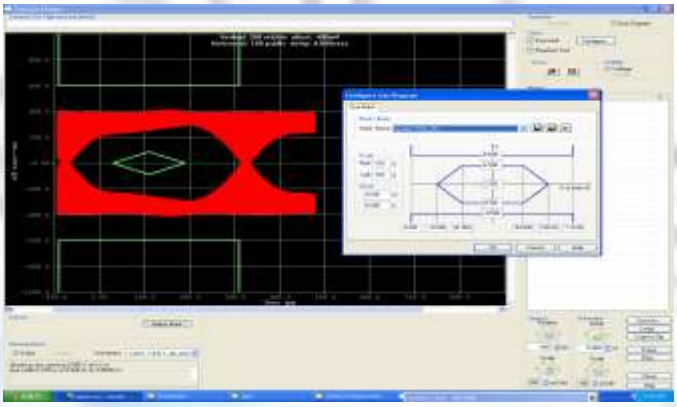

Fig 10: Eye diagram PCIe Receiver at 2.5GT/s

IV. CONCLUSION

The signal integrity issues observed has been solved using HyperLynx signal integrity tool. The comparative result shows that by proper stack up, control impedance technique and reducing dielectric thickness Signal Integrity can be improved. And the Eye Diagram (eye pattern) is used to analyze the Quality and timing of High speed serial data.

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