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Low power full adder design and power analysis

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ABSTRACT: In this paper, various designs of low-power full-adder cell are studied. Simulation of these full-adder cells are carried out. The experiments simulate all combinations of input transitions and consequently determine the power consumption for the various full-adder cells. The simulation results highlight the weaknesses and the strengths of the various full-adder cell designs. The high performance low power full adder circuit is designed and the simulation has been carried out on Tanner EDA tool. The result shows that the proposed high performance low power full adder is an efficient full adder cell with least MOS transistor count that reduces the high power consumption and it considerably increases the speed.

Keywords: Full-adder cell design, low-power circuits, power and delay estimation, VLSI implementations.

1. INTRODUCTION

Low power circuit design has been a challenge for a long time and it is now one of the most important goals of today's CMOS designs. Signal processing is one of the most power hungry applications. Adders are the main building blocks for signal processing applications. Saving power in adders would reduce the power consumption significantly at the chip level. Low power can be achieved at four different levels of the design process, the architectural, the circuit, the device or the layout levels. Power consumption in CMOS digital circuits [1] is divided into three major components as follows:

$$P_{tot} = P_{dynamic}\,(P_d) + P_{static} + P_{short\ circuit}$$

The dynamic component is the part of power consumed when the circuit is switching from one state to another. To be able to estimate the worst case or max power consumption, we need to exhaustively switch the circuit through all of its states. The basic dynamic power consumption of a conventional CMOS digital circuit is given by:

$$Pd = \alpha * f * V_{dd}^{\ 2} * C_{load}$$

- α: is the activity factor which represents the switching activity of the cell on a probabilistic/statistical basis. This is the same for all simulations for all circuits so it is a don't care for relative power consumption analysis.
- f: frequency of switching the input signals. This is considered as the max frequency of the inputs.
- Vdd is the positive supply voltage.
- Cload: is the load on the output node. This is the same for all circuits.

At the device level, reducing the positive supply voltage Vdd and reducing the threshold voltage accordingly would reduce the power consumption significantly. At the layout level, some tricks can be used including the use of short smaller transistors, poly and diffusion areas and the use of shorter metal lines for connections of different devices. These mainly reduce the loading i.e. parasitic capacitances in different parts of the device and circuit. At the design level, different methodology to achieve the required function such as CPL instead of traditional CMOS, can reduce area and consequently power. On an architecture level, an algorithm that requires less or smaller gates, maybe minimizing all circuits on an architectural level, can be used to reduce the overall power consumption.

2. DETAILS OF PAPER

A. Dynamic Differential Cascade Voltage Switch Logic- DDCVSL

Dynamic DCVSL [8], is a combination between the domino logic and the static DCVSL. Circuit diagram of the dynamic DCVSL full adder is given in Figure 1. The advantage of this style over domino logic is the ability to generate any logic function. Domino logic can only generate non inverted forms of logic. For example, in the design of a ripple carry adder, two cells are to be designed for the carry propagation, one for the carry signal and another for the complementary one (in Figure 1), the cell for the true carry signal is only shown, but the one for the complementary signal is also required).Using DCVSL to design dynamic circuits will eliminate p-logic gates because of the inherent availability of complementary signals. The p-logic gates usually cause long delay times and consume large areas.

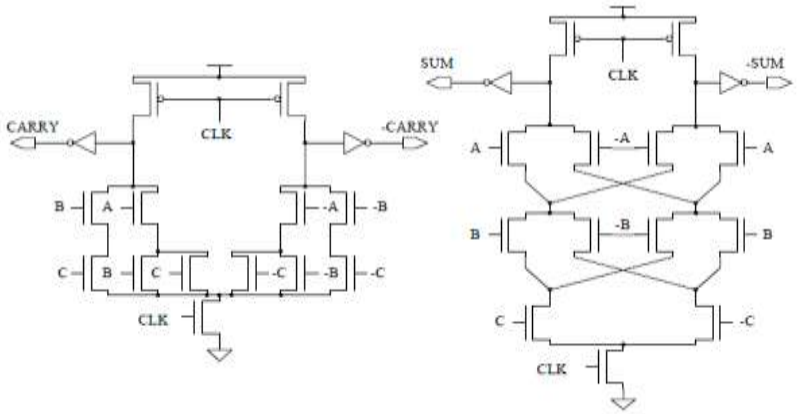

Fig 1: DDCVSL logic circuit

B. Static Differential Cascode Voltage Switch Logic -SDCVSL

Static DCVSL [7], is a differential style of logic requiring both true and complementary signals to be routed to gates. Figure 2 shows the diagram of the static DCVSL full adder. Two complementary nMOSFET have switching trees which are constructed to form a pair of cross-coupled pMOSFET transistors. Depending on the differential inputs one of the outputs is pulled down by the corresponding nMOSFET network. The differential output is then latched by the cross-coupled pMOSFET transistors. Since the inputs drive only the nMOSFET transistors of the switching trees, the input capacitance is typically two or three times smaller than that of the conventional static CMOS logic.

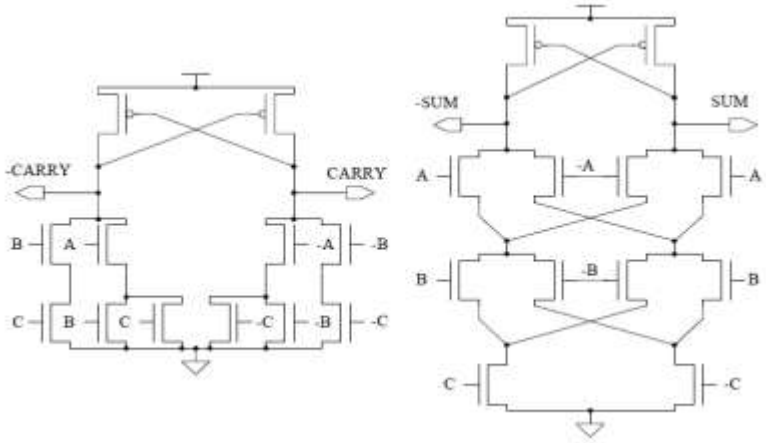

Fig 2: SDCVSL logic circuit

C. Static Differential Split-level Logic - SDSL

The SDSL full adder circuit diagram is given in Figure 3. Two nMOSFET transistors with their gates connected to a reference voltage (Vref = (Vdd/2) + Vthn, Vthn: nMOSFET threshold voltage) are added to reduce the logic swing at the output nodes. Output nodes are clamped to half of the supply voltage level. Thus, the circuit operation becomes faster than the standard DCVSL circuits. However, due to incomplete turn-off of the cross-coupled pMOSFET transistors, SDSL circuits dissipate high static power dissipation. Also, the addition of two extra nMOSFET transistors per gate results in area overhead.

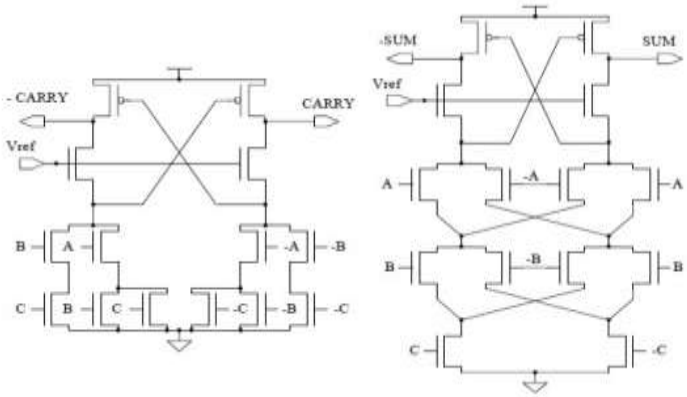

Fig 3: **SDSL logic circuit**

3. TANNER OUTPUT

All the three types of adder designs are simulated on TANNER EDA and their waveforms are plotted . Power analysis of all these three full adder designs are simulated on 90nm and 32nm technology.

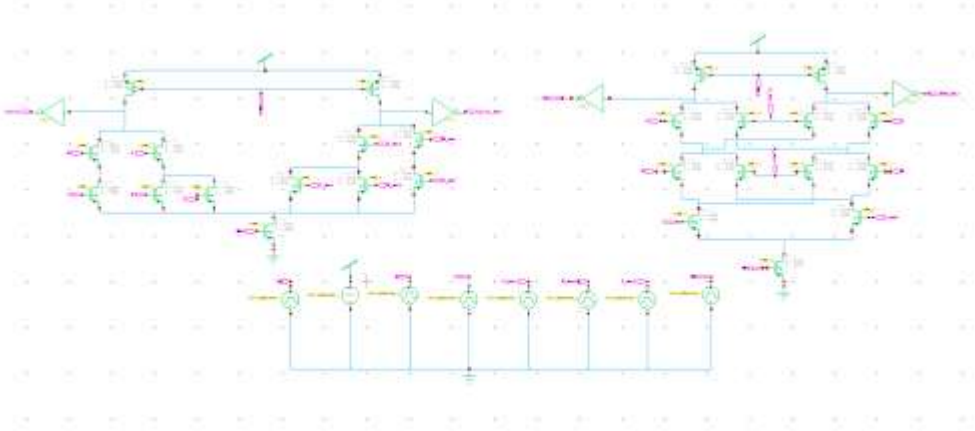

Fig 4: DDCVSL schematic

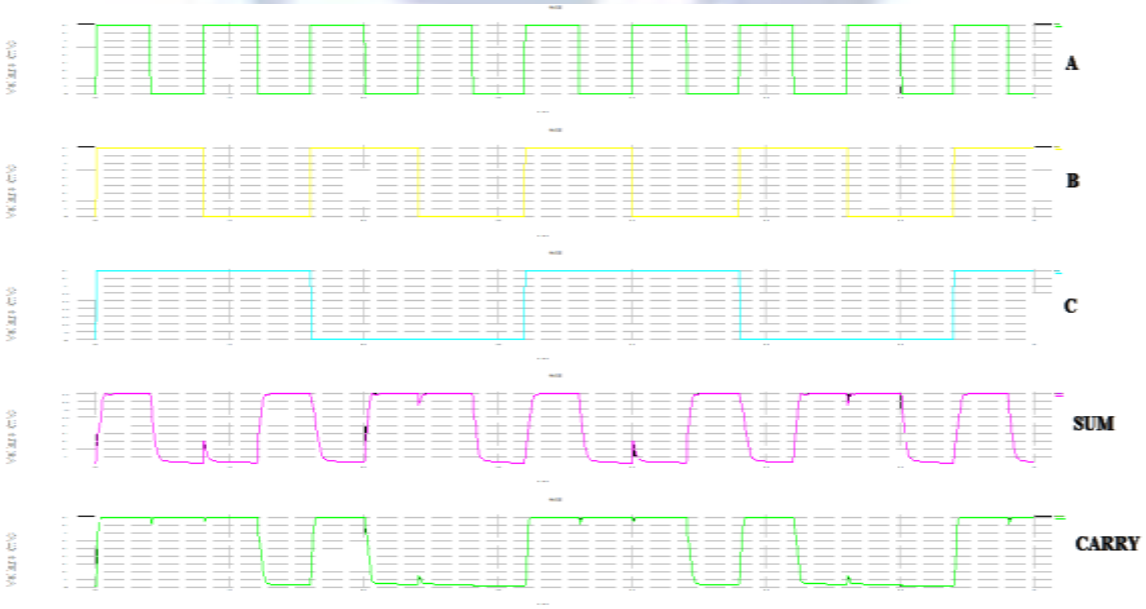

Fig 5.DDCVSL waveform

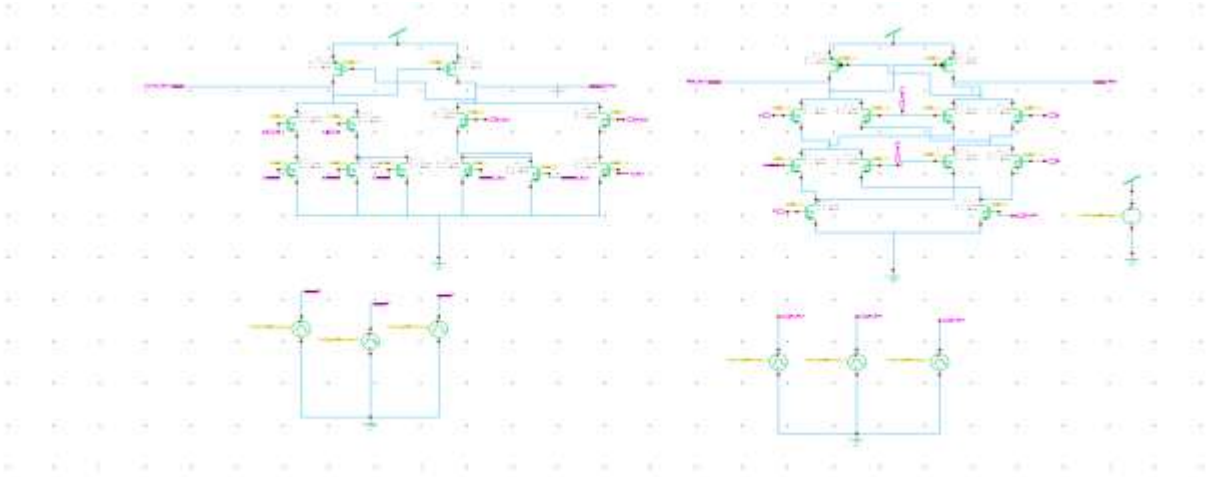

Fig 6: SDCVSL schematic

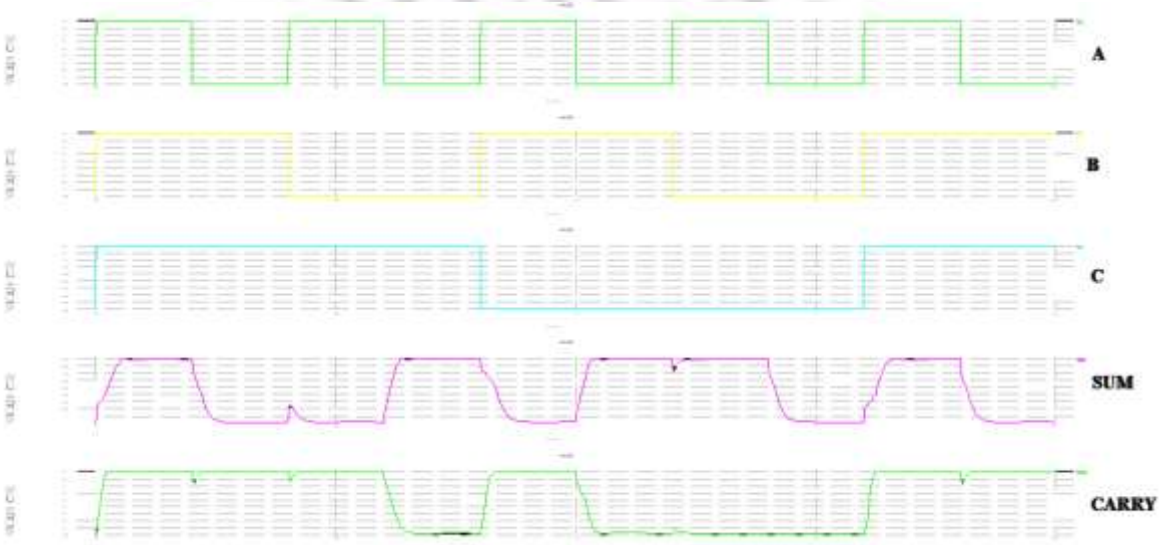

Fig 7. SDCVSL waveform

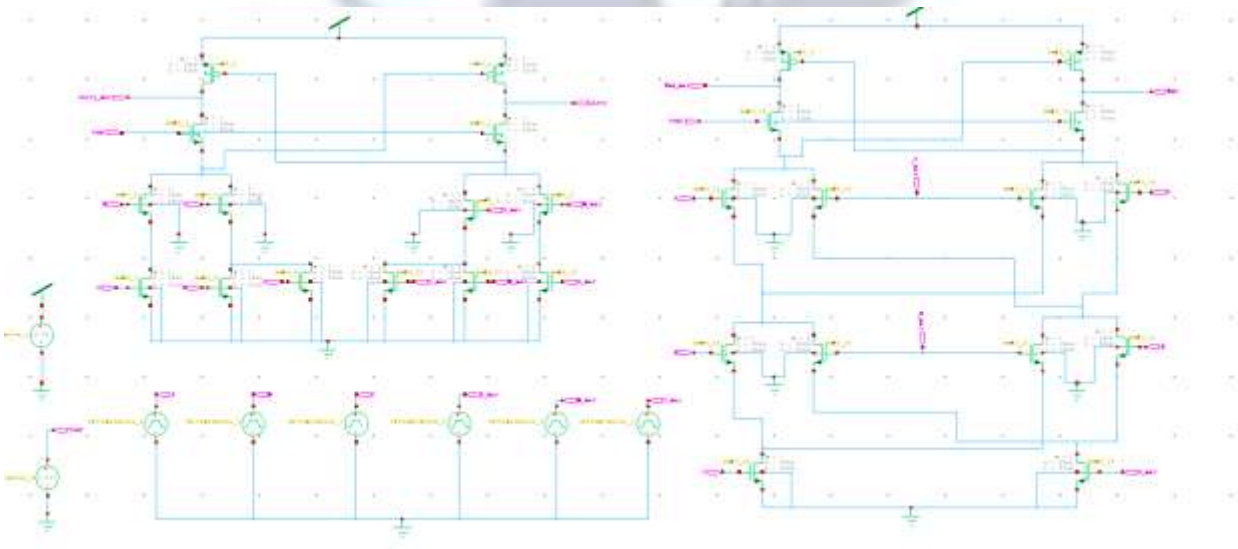

Fig 8. SDSL schematic

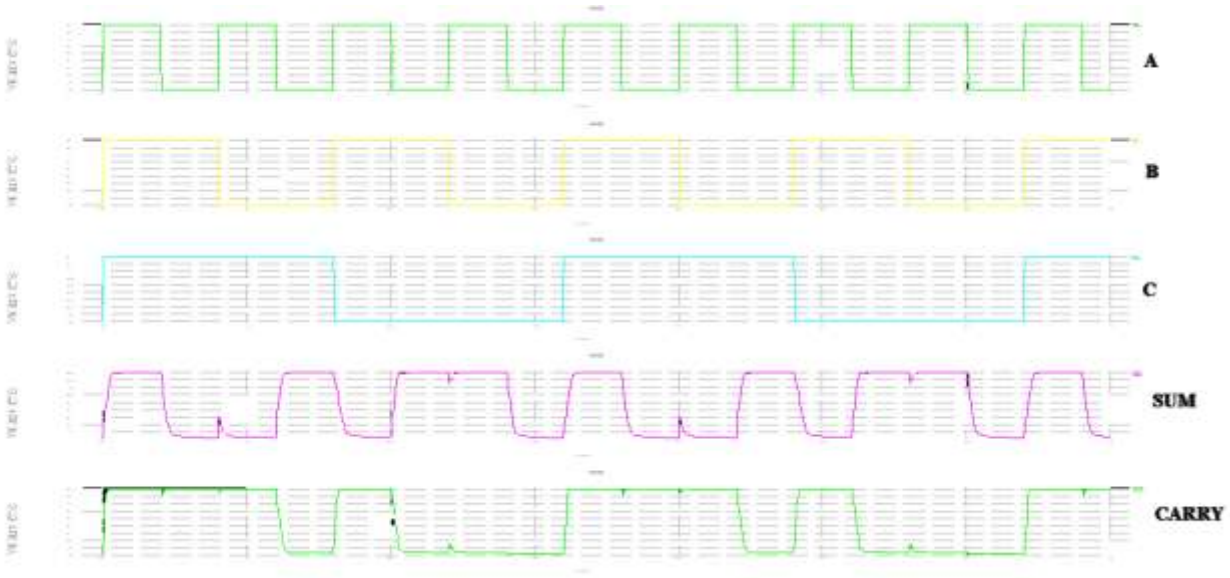

Fig 9. SDSL waveform

4. CONCLUSION

Graph

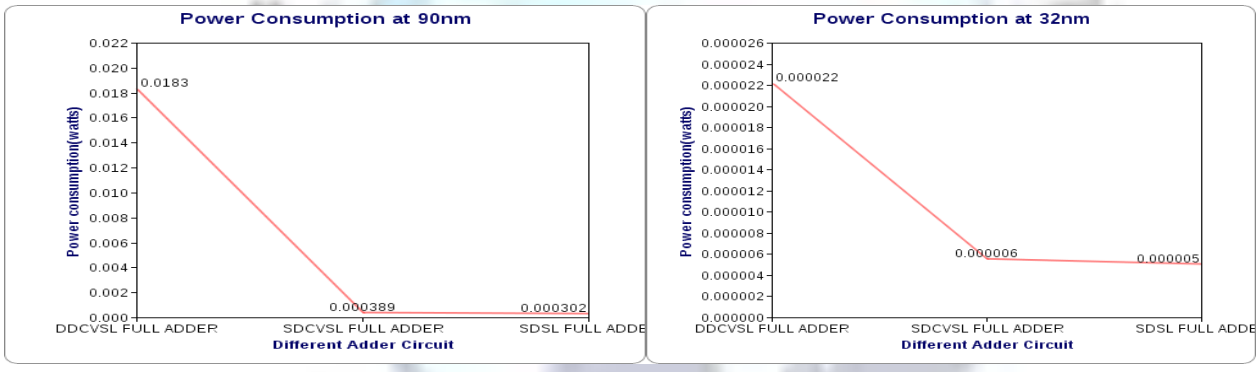

Table containing the values of power dissipation for all the three designs are plotted below

Low Power Full Adder	POWER CONSUMPTION AT DIFFERENT TECHNOLOGY	
	90nm Tech	32nm Tech
DDCVSL FULL ADDER	1.83 X 10^{-2} watts	2.22 X 10^{-5} watts
SDCVSL FULL ADDER	3.89 X 10^{-4} watts	5.54 X 10^{-6} watts
SDSL FULL ADDER	3.02 X 10^{-4} watts	5.05 X 10^{-6} watts

From the above observation it is clear that as the length of transistor used in particular full adder cell increases power consumption also increases. We have taken here the optimum width at which the power consumption is minimum as shown in table. It can be also seen from table that DDCVSL FULL ADDER cell has higher dissipation than SDSL FULL ADDER cell has the least power dissipation of the three.

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