

FPGA Implementation of Low Power and Area Efficient Carry Select Adder

A. Nithya¹, A. G. Priyanka², B. Ajitha³, D. Gracia Nirmala Rani⁴, S. Rajaram⁵

^{1,2,3}Student, ⁴Assistant Professor, ⁵Associate Professor

^{1, 2,3,4,5}Department of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai, India

Abstract: In this paper, we have proposed a modified carry select adder which is known as fastest adders that can perform arithmetic operations in Digital signal processors. Modification in the gate level of the Square root Carry Select Adder (SQRT CSLA) structure results in the reduction of area and power of the CSLA structure which offers a simple and efficient function. Depending upon the Regular SQRT CSLA, we have modified the structure of the adders. The proposed design for 128-bit modified CSLA has reduced area and power as compared with the regular SQRT CSLA with only a slight increase in the delay. The experimental result shows that the proposed CSLA structure is better than the regular SQRT CSLA.

Keywords: Application-specific integrated circuit (ASIC), Carry Select Adder (CSLA), low power.

I. INTRODUCTION

Design of area and power efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input $C_{in} = 0$ and $C_{in} = 1$, then the final sum and carry are selected by the multiplexers (mux)

The basic idea of this paper is to use Binary to Excess-1 Converter (BEC) instead of RCA with $C_{in} = 1$ in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n -bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section B. This paper is structured as follows.

The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented in Sections II and III, respectively. The ASIC implementation details and results are analyzed in Section IV. Finally, the work is concluded in Section V.

A. THE BASIC ADDER BLOCKS

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Fig. 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay.

The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

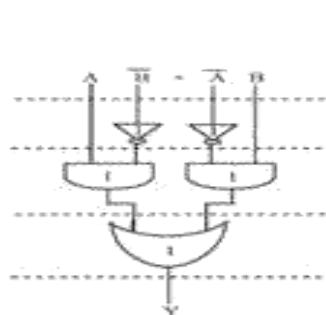


Fig. 1. XOR gate.

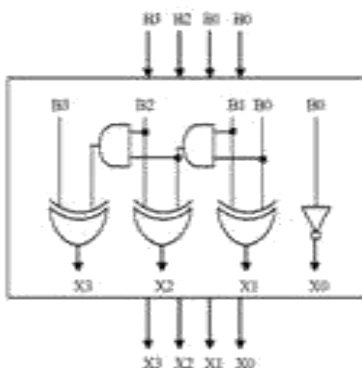


Fig. 2. 4-b BEC unit

Table I Delay and Area Count of the Blocks of CSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

B. BEC

As stated above the main idea of this work is to use BEC instead of the RCA with $C_{in}=1$ in order to reduce the area and power consumption of the regular CSLA. To replace the n -bit RCA, an $n+1$ -bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig. 2 and Table II, respectively. Fig. 3 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as its input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal C_{in} . The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed.

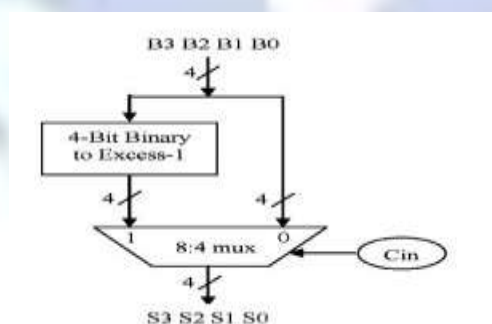


Fig. 3. 4-b BEC with 8:4 mux

Table II Function Table of The 4-B Bec

B[3:0]	X[3:0]
0000	0001
0001	0010
:	:
:	:
1110	1111
1111	0000

II. REGULAR 128-B SQRT CSLA

The structure of the 128-b regular SQRT CSLA is shown in Fig. 4. It has five groups of different size RCA. The delay and area evaluation of each group are shown in Fig. 5, in which the numerals within specify the delay values, e.g., sum2 requires 10 gate delays. The steps leading to the evaluation are as follows.

i) The group2 [see Fig. 5(a)] has two sets of 2-b RCA. Based on the consideration of delay values of Table I, the arrival time of selection input C_1 is earlier than s_3 and later than s_2 . Thus, sum_3 is summation of s_3 and the corresponding mux and sum_2 is summation of C_1 and its corresponding mux.

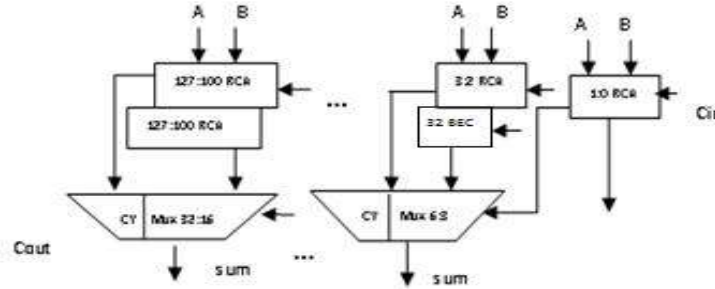


Fig. 4: 128-b SQRT CSLA

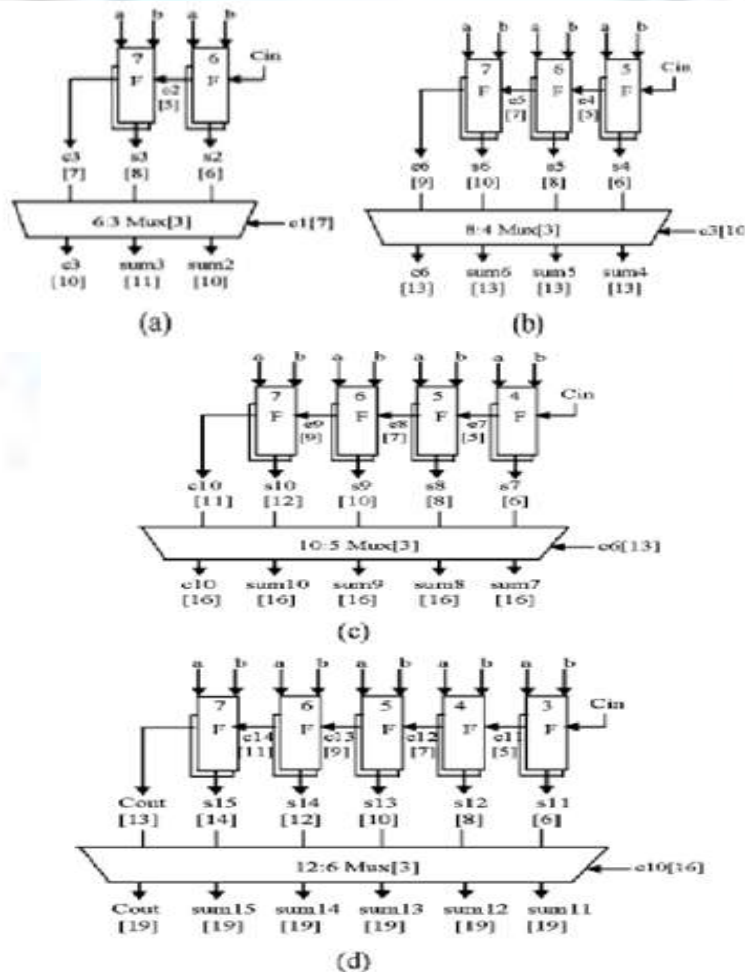


Fig. 5. Delay and area evaluation of Regular SQRT CSLA (a)group 2, (b)group3, (c)group4, (d)group 5

ii) Except for group2, the arrival time of mux selection input is always greater than the arrival time of data outputs from the RCA's. Thus, the delay of group3 to group5 is determined, respectively as follows:

$$\begin{aligned}\{c6, \text{sum}[6:4]\} &= c3[t=10] + \text{mux.} \\ \{c10, \text{sum}[10:7]\} &= c6[t=13] + \text{mux.} \\ \{c_{out}, \text{sum}[15:11]\} &= c10[t=16] + \text{mux}\end{aligned}$$

iii) The one set of 2-b RCA in group2 has two FA for $C_{in} = 1$ and the other set has 1 FA and 1 HA for $C_{in} = 0$ based on the area count .

iv) Similarly, the estimated maximum delay and area of the other groups in the regular SQRT CSLA are evaluated and listed in Table III.

Table III: Delay And Area Count Of Regular SQRT CSLA Groups

Group	Delay	Area
Group 2	11	57
Group 3	13	87
Group 4	16	117
Group 5	19	147

The total number of gate counts in group2 is determined as follows:

$$\text{Gate count} = 57(\text{FA} + \text{HA} + \text{MUX})$$

$$\begin{aligned}\text{FA} &= 39(3*13) \\ \text{HA} &= 6(1*6) \\ \text{MUX} &= 12(3*4)\end{aligned}$$

III. MODIFIED 128-B SQRT CSLA

The structure of the proposed 128-b SQRT CSLA using BEC for RCA with $C_{in}=1$ to optimize the area and power is shown in Fig. 6. We again split the structure into five groups. The delay and area estimation of each group are shown in Fig. 7. The steps leading to the evaluation are given here.

i) The group2 [see Fig. 7(a)] has one 2-b RCA which has 1 FA and 1 HA for $C_{in}=0$. Instead of another 2-b RCA with $C_{in}=$, a 1b BEC is used which adds one to the output from 2-b RCA.

ii) For the remaining group's the arrival time of mux selection input is always greater than the arrival time of data inputs from the BEC's. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

(iii) The area count of group2 is determined as follows:

$$\text{Gate count} = 43(\text{FA} + \text{HA} + \text{MUX} + \text{BEC})$$

$$\begin{aligned}\text{FA} &= 39(3*13) \\ \text{HA} &= 6(1*6) \\ \text{AND} &= 1 \\ \text{NOT} &= 1 \\ \text{XOR} &= 10(2*5) \\ \text{MUX} &= 12(3*4)\end{aligned}$$

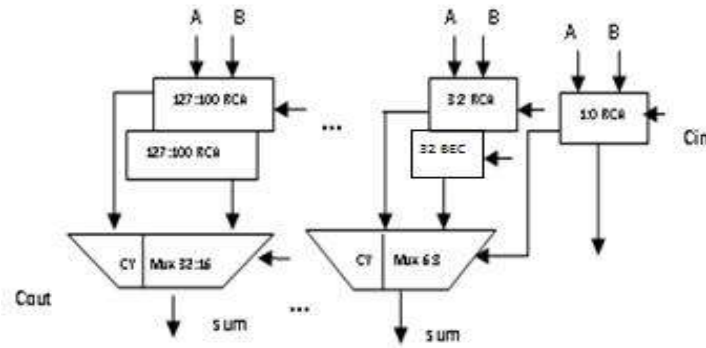
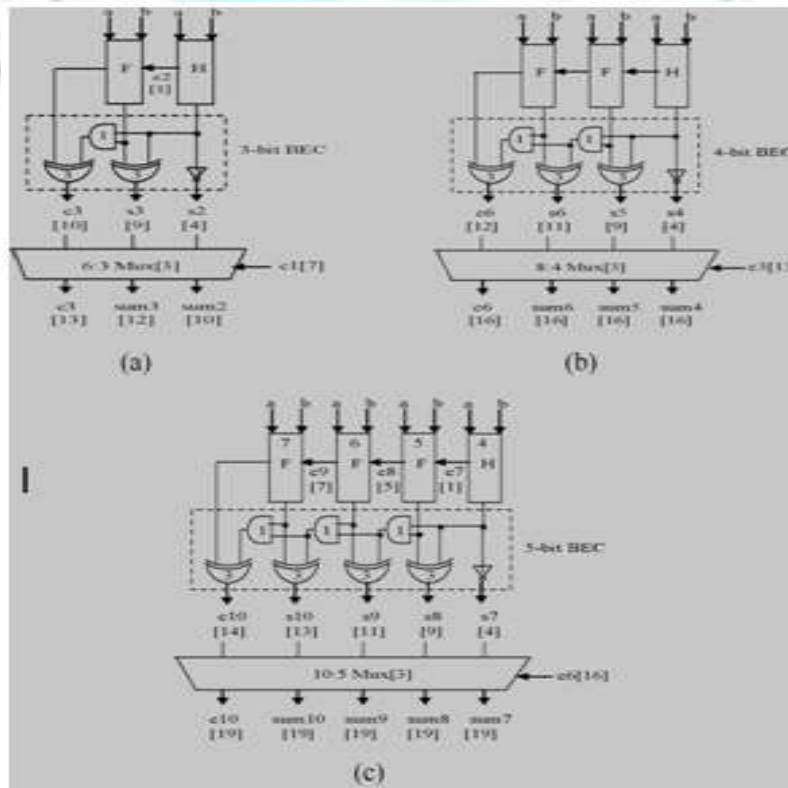


Fig.6. Modified 128-b SQRT-CSLA

4) Similarly, the estimated maximum delay and area of the other groups of the modified SQRT CSLA are evaluated and listed in Table IV.

Table IV. Delay And Area Count Of Modified Sqrt Csla

Group	Delay	Area
Group 2	13	43
Group 3	16	61
Group 4	19	84
Group 5	22	107



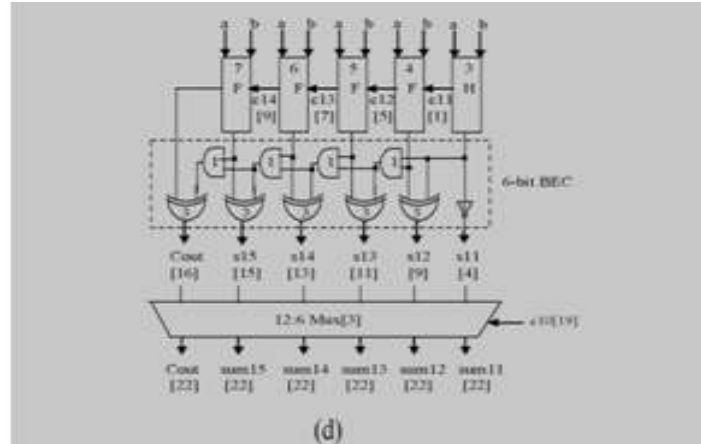


Fig.7. Delay and area evaluation of modified Sqrt CSLA: (a) group 2 (b) group 3 (c) group 4 and (d) group 5. H is a Half Adder

IV. SIMULATION RESULTS

The proposed design has been developed using Verilog-HDL and simulation is done by Xilinx ISE 14.1 simulator. The comparison of area, delay and power between Regular CSLA and Modified CSLA for 16-bit, 32-bit and 128-bit are shown in Table V.

The area indicates the reduction in number of gates in the modified Sqrt CSLA and the total power is sum of the leakage power, internal power and switching power. Compared to the regular CSLA the number of gates have been reduced in the modified CSLA therefore there is reduction in the area of the modified CSLA

Table V. Comparison of Values

Bit	Regular		Modified	
	Area(no. of gates)	Power	Area(no. of gates)	Power
16	348	315	291	268
32	698	553	762	448
128	1976	960	1948	864

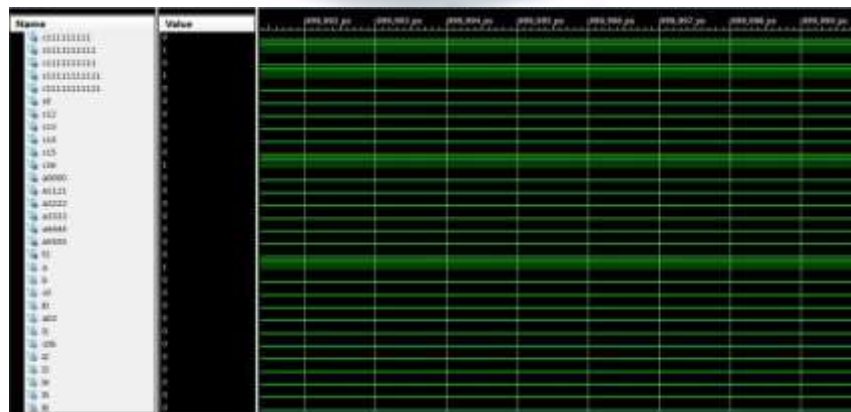


Fig .8: Regular Sqrt CSLA

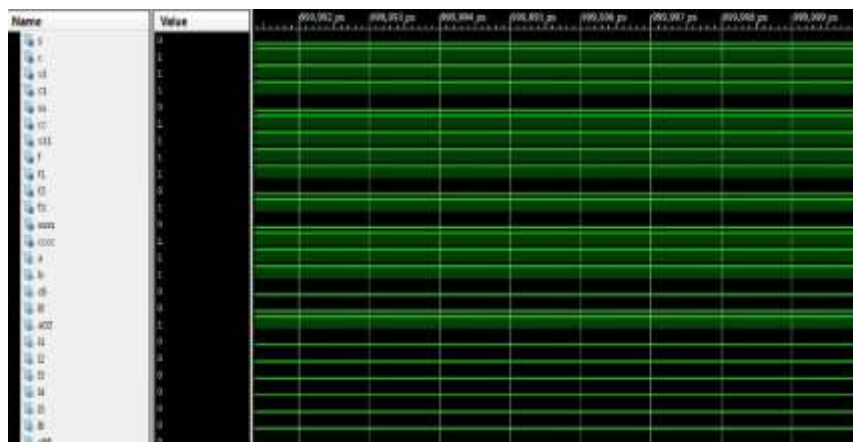


Fig.9: Modified SQRT CSLA

V. CONCLUSION

Adders can be constructed for many numerical representations, such as BCD or Excess-1, the most common adders operate on binary numbers. In this paper, we have designed adders using Binary Excess-1 convertors. CSLA can be used for high speed multiplications, they are also used in Advanced Microprocessor design. The reduced number of gates in the modified 128 bit SQRT CSLA offers the great advantage in the reduction of area, delay and also the power. The future scope of this work is to implement 256- bit SQRT CSLA. It would be interesting to test the design of the modified for 256-b.

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