International Journal of Enhanced Research in Science Technology & Engineering, ISSN: 2319-7463
Vol. 3 Issue 2, February-2014, pp: (237-241), Impact Factor: 1.252, Available online at: www.erpublications.com

Power and delay efficient Full Adder Design for various technology

Vicky Kanoji[1], Anjana R[2]
[1]UG Student LIT, Sarigam, Gujarat, India
[2]Research Scholar, Dr. K. N Modi University, Gujrat, India

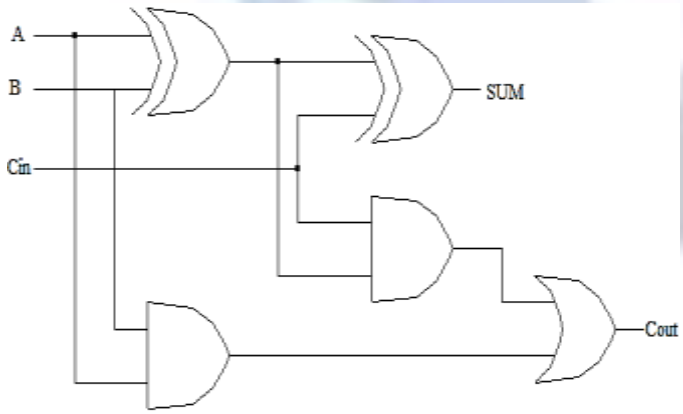
Abstract: This paper presents a comparison of different adder circuit based on logic design and Technology used to fabricate it. The performance there adders are measured in terms of area, delay and power. Adders are the most critical part of the ALU and used for many arithmetic operations. We have tested the various adders such as Half Adder, Full Adder, Ripple Carry Adder (RCA) and Full Adder using Mux (2x1) on DSCH2 and Microwind 3.1. The experiment is performed on 32nm, 45nm, 90nm and 180um Tech with 1.2v supply Voltage. Adders can also be implemented using MUX, but there is area and delay overhead with minimum power reduction.

Keywords: Full Adder, Half Adder (HA), RCA, Full Adder using MUX, Power, Delay, Area, Comparison based on technology.

Introduction

Most of the processor, digital system contains many data path circuits. Adders are one among them and mostly used one. Adders not only performs arithmetic addition but is also used in other arithmetic operations such as subtraction, Division and multiplication. Thus researchers have now focused on this circuit so that one can squeeze out the maximum performance from this adder.

Full Adder is a combinational circuit that performs addition of two bits along with carry Cin produced in the previous stage. The logical diagram of the Full Adder is as shown in Fig. 1. The truth table for the given combinational circuit is as given in table.



A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

Figure 1. Logic Diagram Of Full Adder With Its Truth Table.

Moreover there are varieties of adders such as Ripple Carry Adder, Carry Look Ahead Adder, Carry Select Adder, Carry Skip Adder, Carry Bypass Adder used according to the requirement.

Comparison between different Adders

A. Half Adder:

Half Adder is a basic combinational circuit that performs addition of two single bit binary digits. After addition operation, it produces two operation sum and carry. The logic diagram and its Boolean equation are given below:

Sum = A EX-OR B

Cout = A AND B

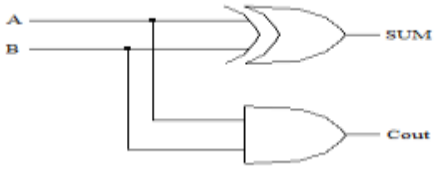


Figure 2. Half Adder.

A. Full Adder:

Full Adder is a combinational circuit that performs addition operation on three single bit binary digits. It produces two operation sum and carry. The Boolean equation is given below:

Sum = A EX-OR B EX-OR C

Cout = (A EX-OR B) Cin + A AND B

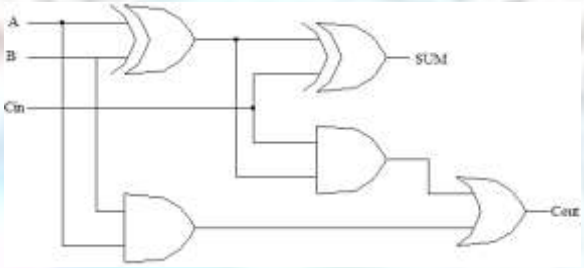


Figure 3. Full Adder

Here Cin is a carry in bit. [The carry produced by the addition of previous stage]. Whereas A & B are the two operands on which addition is performed. Full Adder is a fundamental block for any complex adder. Thus the Full Adder circuit should be a power efficient, low area and having minimal delay. [2]

Complex Adders

A. Ripple Carry Adders (RCA):

To add 'n' bit of binary digit we have to use 'N' number of Full Adder circuit. Since the carry generated by I-Stage is passed on to the II-Stage, i.e. the carry ripples from I-Stage to the last stage. This circuit is known as "Ripple Carry Adder". Even though it is faster in regard with time, it is relatively slower, since each Full Adder stage has to wait for the carry being calculated by the previous stage. The block diagram of 4-bit RCA is shown below: [3]

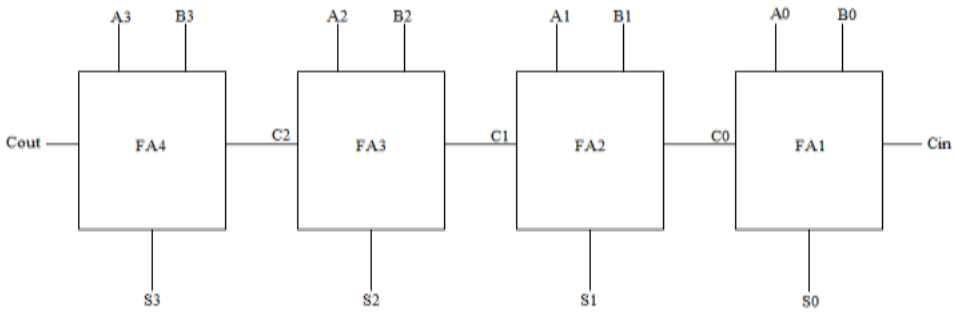


Figure 4. Block Diagram Of Regular 4-Bit Ripple Carry Adder.

A. Full Adder Using MUX:

Full Adder can also be implemented by using 2x1 MUX. By using MUX the delay generated by conventional Full Adder can be reduced, as MUX are faster in operation.

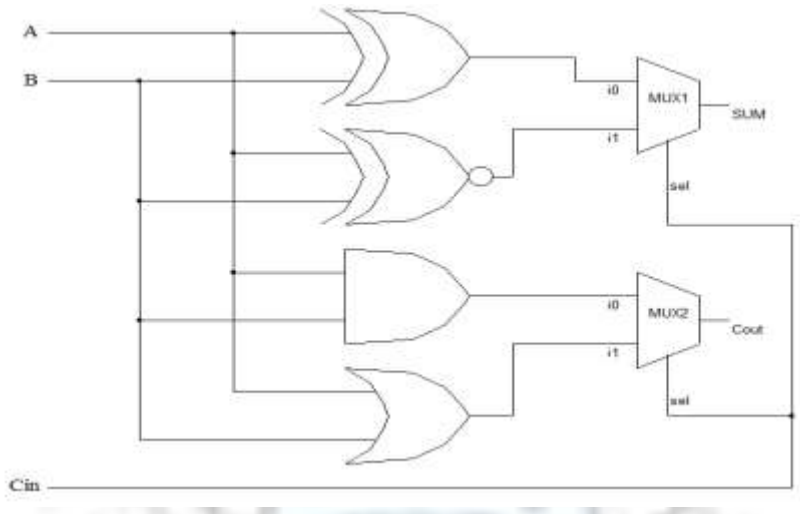


Figure 5. Full Adder Using 2(2x1) Mux.

The combinational circuit for the Full Adder using MUX is as shown in figure. The select line applied to both the MUX (2x1) is common i.e. Cin binary bit A & B are two binary single bit operands on which addition operation is performed. The output of MUX1 provides us with sum and that of MUX2 gives out the carry out bit.

A Carry Select Adder (CSLA):

CSLA is used in many computation circuits to rectify the problem of delay caused due to carry propagation as in RCA the carry ripples from the I-Stage to the n^{th} stage. The CSLA produces multiple carries and then computes the sum on the basis of selected carry. [1]

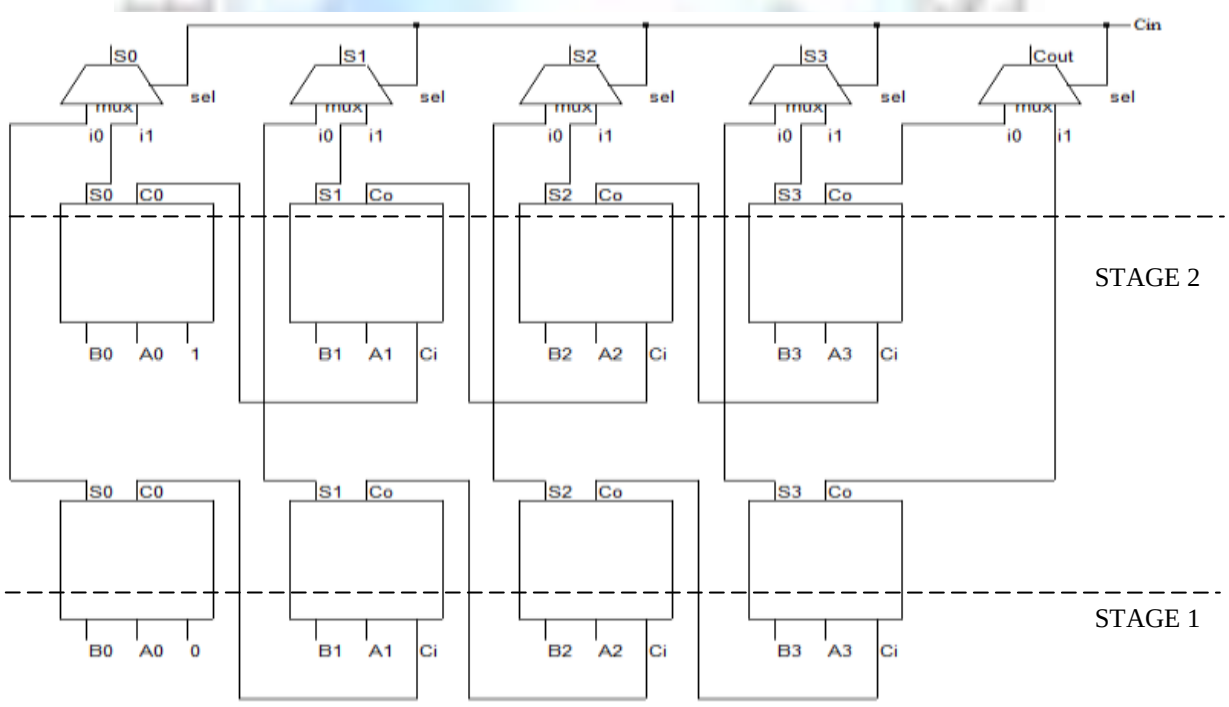


Figure 6. 4-Bit Carry Select Adder

CSLA is not an area efficient adder but it has minimal delay. Moreover it uses RCA to generate the partial sum with Cin=0 in 1^{st} STAGE and Cin=1 in 2^{nd} STAGE. In the final stage MUX is being used to generate the final sum and carry bits. [4]

Experimental Results

Table 1: Comparison of Adders on Basis of Different Technology

TECHNOLOGY	Half Adder			Full Adder			Full Adder using MUX		
	Power	Delay (ps)	Area	Power	Delay (ps)	Area	Power	Delay (ps)	Area
32nm	0.105	29	0.0391	0.235	29.5	0.118	0.298	27	0.985
45nm	0.135	33	0.0956	0.304	46	0.288	0.415	48	2.405
90nm	26.647	9.5	1.53	65.712	11	4.609	39.371	10	38.48
180um	35.033	41.5	24.49	85.435	53.5	73.75	81.925	56	615.68

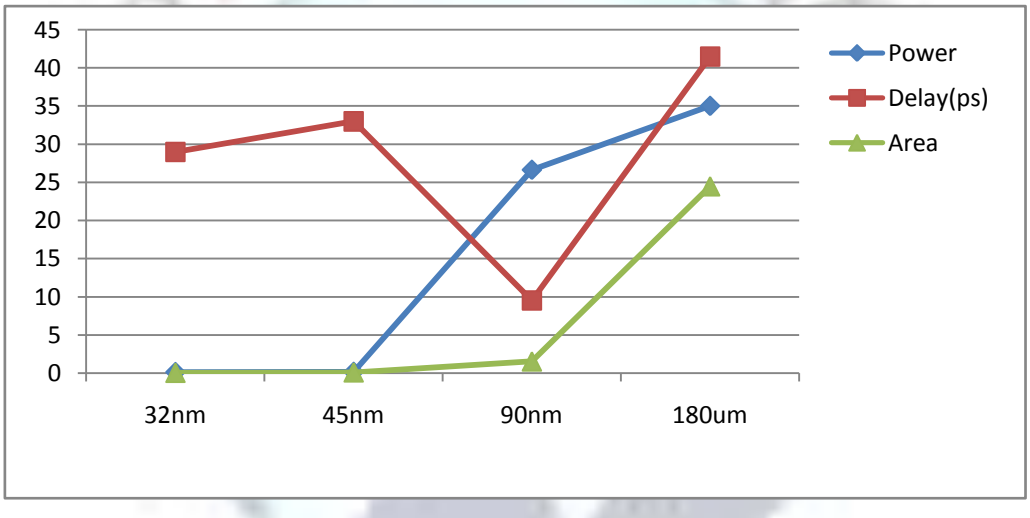


Figure 7. Graphical Analysis of Of Half Adder.

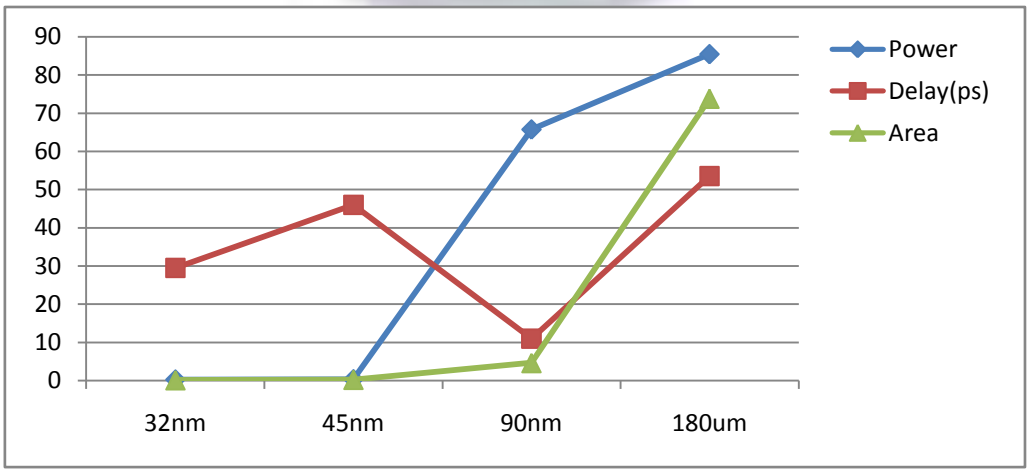


Figure 8. Graphical Analysis of Parameters Of Full Adder.

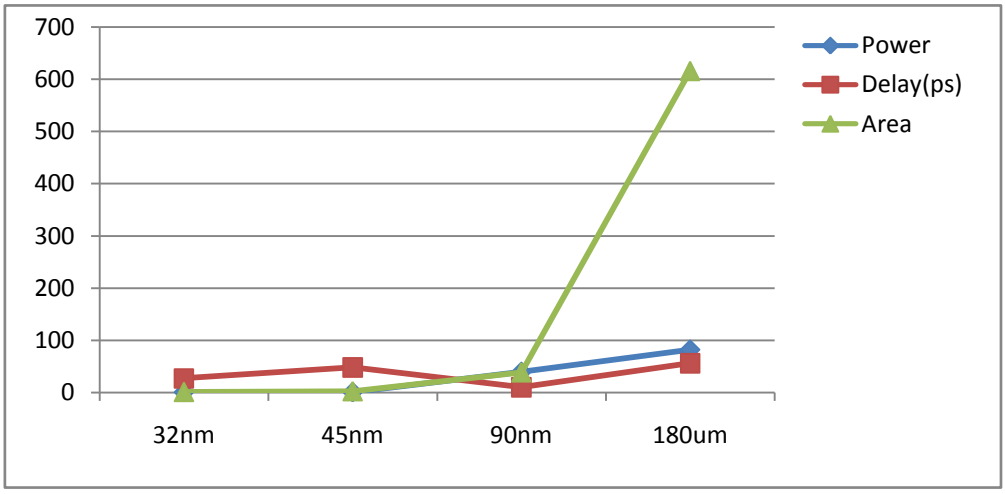


Figure 9. Graphical Analysis of Full Adder Using MUX.

Conclusion

In this proposed paper we have successfully compared various adders on basis of power, delay and area. The Full Adder using MUX can be used for faster operation and low power consumption with area overhead. The Full Adder Using MUX shows 40% and 9% reduction in area and delay respectively with respect to Regular Full Adder when Fabricated using 90nm Technology. Moreover we can conclude that we can use the Full Adder using MUX for the construction of RCA and CSLA in place of regular Full Adder, so that the Delay and Power gets minimized.

References

[1]. O. J. Bedrij,"Carry Select Adder" IRE Trans. Electron. Comput., pp. 340-344, 1962.

[2]. Saranindu Panda, a. Banerjee, B. Maji, Dr. A. K. Mukhopadhyay, "Power and Delay Comparison in between Different tyoes of Full Adder Circuits", IJAREEIE, Vol. 1, Issue 3, Sept. 2012.

[3]. Rajender Kumar, Sandeep Dahiya,"Performance Analysis of Different Bit Carry Look Ahead Adder Using VHDL Environment", IJESIT, Vol. 2. Issue 4, July 2013.

[4]. P. Gurjar, R. Solanki, O. Kansliwal, M. Vucha,"VLSI Implementation of Adders for High Speed ALU", IJCA (0975-8887), Vol. 29- No. 10, Sept. 2011.

[5]. B. Ramkumar and Harish M Kittur, "Low-Power and Area-Efficient Carry Select Adder", IEEE transaction on VLSI Systems, VOL. 20, NO. 2, February 2012.

[6]. T. Y. Ceiang and M. J. Hsiao, "Carry-select adder using single ripple carry adder," Electron. Lett. vol. 34, no. 22, pp. 2101–2103, Oct. 1998.