

CMOS Implementation of Cascaded Instrumentation Amplifier with DC Offset Voltage Reduction

Ahmad Sadab¹, Mohd. Khursheed Siddiqui², Awill Anurag Misra³, Mohd. Amir Ansari⁴

^{1,3}Research Scholar PG, ²Associate Professor, ⁴Assistant Professor

^{1,2}Dept. of Electrical Engineering, Integral University Lucknow, U.P. – 226026, India

^{3,4}Dept. of Electronics & Communication Engg., Integral University, Lucknow, U.P. –226026, India

Abstract: Op-Amp Instrumentation Amplifier (INA) is one of the most fascinating and widely used devices in analog signal conditioning circuit which amplifies very small differential signal while cancelling the common mode signal. By cascading, we can amplify the signal of Yokto level (10-24) to the saturation level of Op-Amp i.e., if we use the structure of INA with order five, it amplifies the signal upto 490dB at normal conditions of component and approximately 630 dB at critical values of all the components. The problem of dc-offset can be rectified by modified circuit of cascaded INA which restricts the output to be clipped. Although it is very important building block for small signal amplification circuits, with every stage of cascaded INA the size of the circuit increases. In this paper, we present the CMOS implementation of cascaded INA with dc-offset reduction capability. The use of CMOS in INA is gaining nowadays because of its low power requirement. CMOS transistors use little power and do not produce as much heat as the traditional BJT. Since the size of channel length of CMOS transistor is shrinking very significantly, it allows a high density of logic functions on chip. Further we present the hypothesis to implement the cascaded INA with dc-offset reduction using DGMOSFET for extracting best performance, utilizing the most from available resources.

Keywords: Operational Amplifier, Differential Amplifier, Instrumentation Amplifier, Cascaded Structure, Gain, Output Offset Voltage short chanel effect, Double gate MOSFET, drain induced barrier lowering, 2D NEGF, NS-DG MOSFET and double gate carbon nano tube FET.

I. INTRODUCTION

This work describes a novel technique of designing a low noise high gain CMOS instrumentation amplifier. With the increase in need to have a device which not only read a signal from a sensor but also to subtract one voltage level from another and amplify the difference significantly, INA comes into existence. It is one of the most versatile signal processing amplifiers. An INA is used for precision amplification of differential DC/AC signals while rejecting large values of common mode noise. To understand the circuit and working of INA properly one should have a thorough knowledge of op-amp in general and DA is specific because it is a modification of DA. The limitations with the DA, the rejection of the common voltage at the inverting and non-inverting terminals is very much dependent on the external resistors. If, there is any mismatch or a variation in these resistors the rejection of the common mode voltage will not be complete. The gain of the circuit is not easy to adjust. To adjust the gain two or more resistors need to be varied. While keeping their ratio exactly matched, this is almost impossible to achieve. The input impedance of two input terminals is finite. So, the two sources that provide the voltages to be subtracted will have to come from two identical and almost ideal sources. A balance between the two input sources of a very high degree is required. To overcome the above limitations of DA certain modifications were made and INA comes into existence.

II. INSTRUMENTATION AMPLIFIER

An INA [4] is a unique combination of commonly used differential inputs of any op-amp and an additional resistor R_{gain} which introduce control on gain of amplifier. Some other additional characteristics included in INA are very low DC offset,

low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, very high input impedance [5]. INA offer a unique combination of differential inputs, high input impedance, excellent precision and noise specifications.

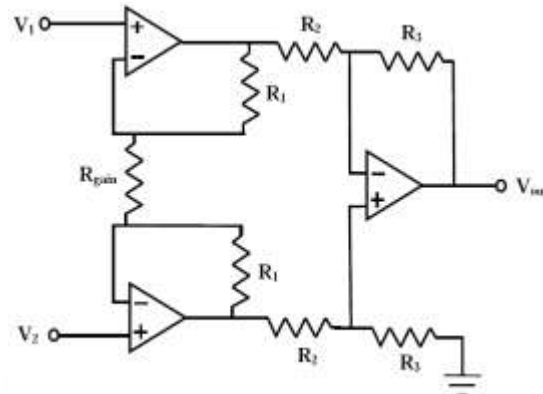


Figure 1. Instrumentation amplifier.

Like all linear technology devices, INAs are unique in offering fully specified, tested and guaranteed performance for key parameters over the full operating temperature range, enabling high reliability designs [6]. An INA is a category of DA that has been united with input buffers, which remove the need for the matching of input impedance and thus make the amplifier appropriate for use in measurement and test equipments. These are arranged, there is one op-amp to buffer each input and one to produce the desired output with adequate impedance matching. The most commonly used INA is shown in the Figure 1. The gain of the INA circuit is,

$$\frac{V_{out}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{gain}}\right) \frac{R_3}{R_2} \quad (1)$$

The differential amplifier circuit [7] demonstrates along with gain R_3/R_2 and differential input resistance $2R_2$. The two amplifiers before the DA are the buffers. When R_{gain} is open circuited, they are simple unity gain buffers; the circuit will work in that condition with gain simply equal to R_3/R_2 and high input impedance. An INA can also be built with two op-amps to save on cost and increase CMRR but the gain must be higher than +6dB. INA without feedback is the high input impedance DA designed, allows lesser number of amplifiers, reduced thermal noise and increased bandwidth.

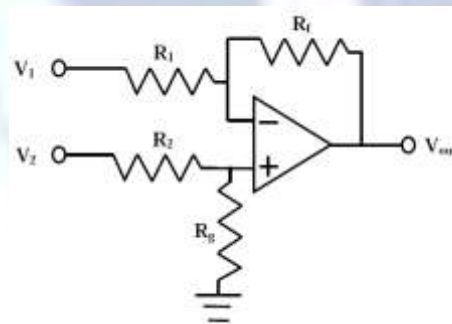


Figure 2. Differential amplifier.

Figure 2 is used for finding the difference of two voltages each multiplied by some constant is also known as DA.

$$V_{out} = \left(\frac{R_f + R_1}{R_g + R_2}\right) \frac{R_g}{R_1} V_2 - \frac{R_f}{R_1} V_1 \quad (2)$$

The input impedance of the DA is approximately $R_1 + R_2$.

CASCADED INSTRUMENTATION AMPLIFIER

The cascaded INA is shown in Figure 3, designed with the help of an additional part of the INA i.e. known as electronically isolated (buffer) circuit, shown in Figure 4. It provides the very high gain by the use of small values of components. The gain for the cascaded INA is,

$$\frac{V_{out}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{gain}}\right) \left(1 + \frac{2R_1}{R_{gain}}\right) \frac{R_3}{R_2} = \left(1 + \frac{2R_1}{R_{gain}}\right)^2 \frac{R_3}{R_2} \quad (3)$$

If, the number of stages is N, the gain for cascaded INA is,

$$\frac{V_{out}}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_{gain}}\right)^N \frac{R_3}{R_2} \quad (4)$$

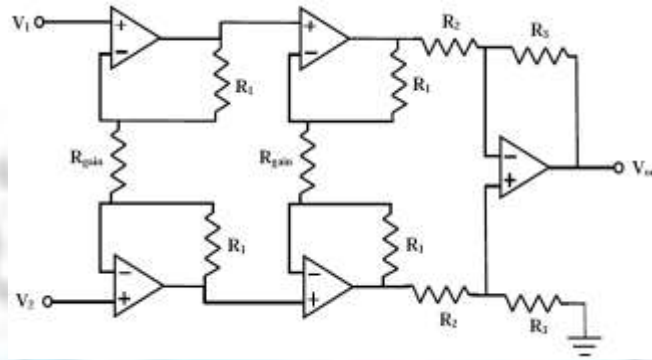


Figure 3. Cascaded instrumentation amplifier.

All the parameters, V_{out} , V_1 , V_2 , R_1 , R_2 , R_3 and R_{gain} are shown Figure 3. If, we increase the number of stages, the gain of the cascaded INA definitely increased with very high rate. Therefore, the cascaded INA concludes that, we can amplify very low level input signals. Therefore, it can be used in different applications as medical instruments, data acquisition systems, electronic measuring instruments, etc but the most important application is noise amplification.

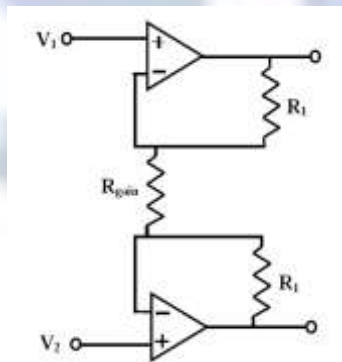


Figure 4. Additional part for the cascaded instrumentation amplifier.

SIMULATION OF CASCADED INA

In Figure 3, the cascaded INA is shown. In equation (4), the general formula of gain for the N stages of INA is given. According to that, Table I represent the typical values of gain and Table II maximum input voltage for the saturation level of cascaded INA at the different ratios of resistances R_3/R_2 and R_1/R_{gain} . The graphical representation of gain is shown in Figure 5 at the different ratios of resistances. Simulation is done through MATLAB simulation software [9], [10].

TABLE I. GAIN (IN dB) OF CASCADED INSTRUMENTATION AMPLIFIER.

No. of stages	Gain (In dB)				
	$R_3/R_2 = R_1/R_{gain} = 1$	$R_3/R_2 = R_1/R_{gain} = 10$	$R_3/R_2 = R_1/R_{gain} = 100$	$R_3/R_2 = R_1/R_{gain} = 1k$	$R_3/R_2 = 1k \text{ \& } R_1/R_{gain} = 10k$
0	0	20	40	60	60
1	9.5424	46.4443	86.0639	126.0249	146.0210
2	19.0848	72.8887	132.1278	192.0498	232.0420
3	28.6272	99.3331	178.1917	258.0748	318.0631
4	38.1697	125.7775	224.2556	324.0997	404.0841
5	47.7121	152.2219	270.3196	390.1247	490.1051

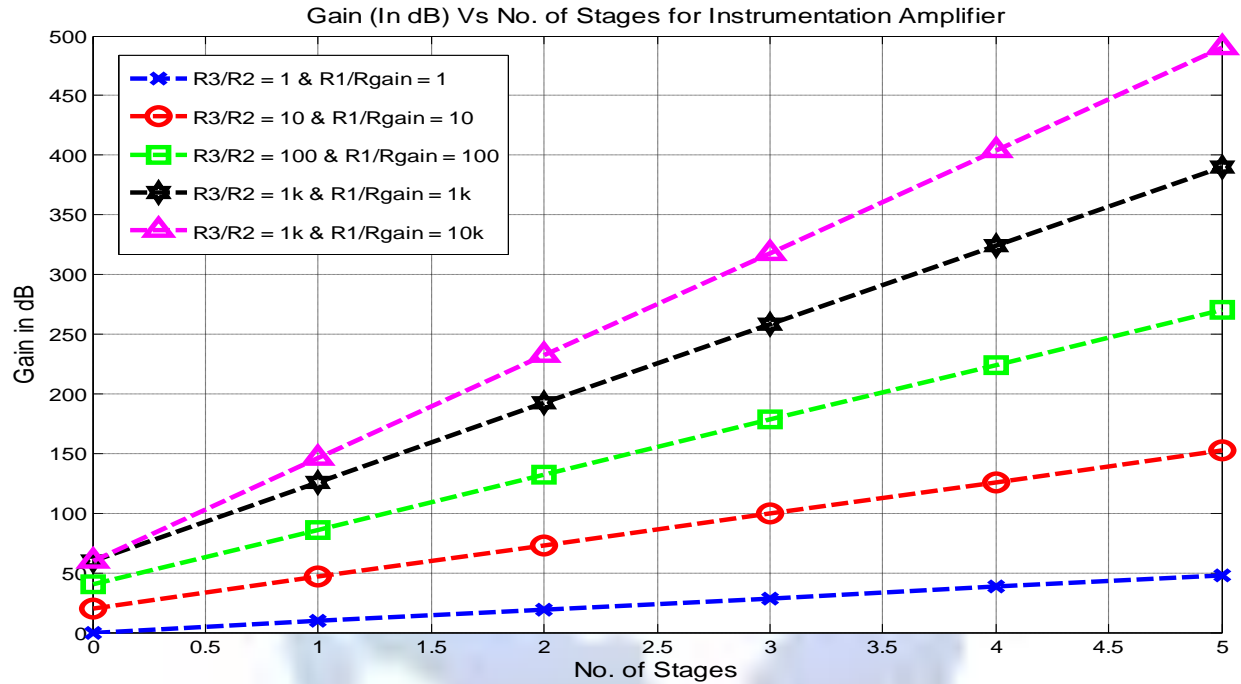


Figure 5. Cascaded instrumentation amplifier gain (in dB) at different values of R_3/R_2 and R_1/R_{gain} .

TABLE II. MAXIMUM INPUT VOLTAGE FOR SATURATION LEVEL OF CASCADED INSTRUMENTATION AMPLIFIER.

No. of stages	Maximum input voltage for saturation level (in Volt)				
	$R_3/R_2 = R_1/R_{gain} = 1$	$R_3/R_2 = R_1/R_{gain} = 10$	$R_3/R_2 = R_1/R_{gain} = 100$	$R_3/R_2 = R_1/R_{gain} = 1k$	$R_3/R_2 = 1k \text{ \& } R_1/R_{gain} = 10k$
0	15	1.5	0.15	0.015	0.015
1	5	0.0714	0.0007	7.496E-06	7.499E-07
2	1.6667	0.0034	3.712E-06	3.746E-09	3.749E-11
3	0.5556	0.0001	1.847E-08	1.872E-12	1.874E-15
4	0.1851	7.712E-06	9.189E-11	9.356E-16	9.373E-20
5	0.0617	3.672E-07	4.572E-13	4.675E-19	4.686E-24

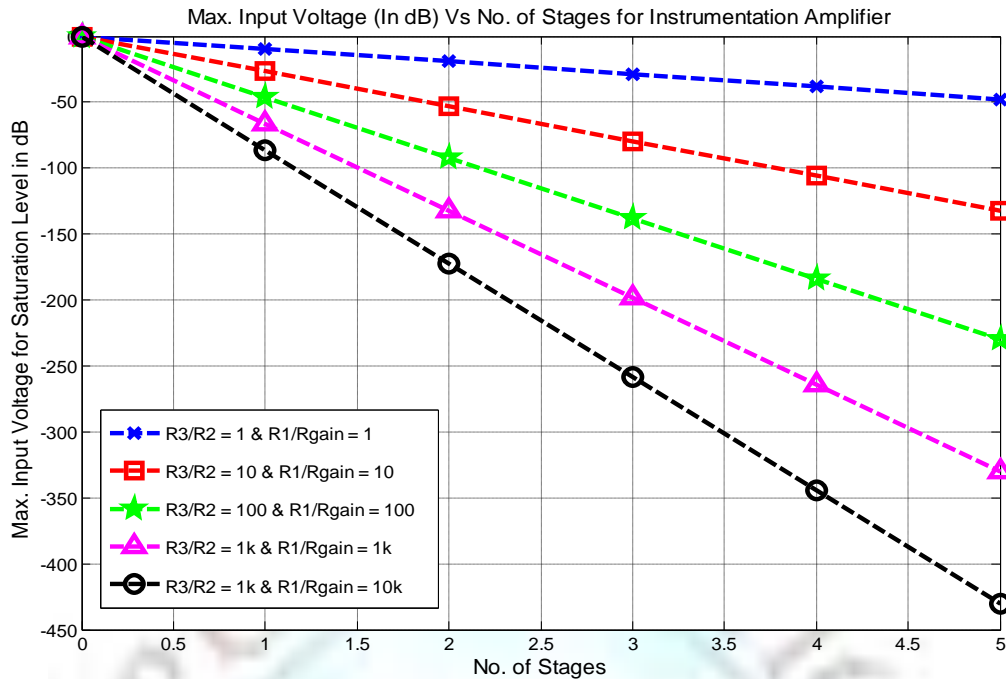


Figure 6. Cascaded instrumentation amplifier maximum input (in dB) w.r.t. zero order INA at different values of R_3/R_2 and R_1/R_{gain} .

Here, the maximum gain level is 490dB at $R_3/R_2=1k$ and $R_1/R_{gain}=10k$ for ideal case upto 5 stages of cascaded INA. It can be increases, if we increase the number of stages. The gain level is approximately 630dB for five stages at the critical values of components. Figure 6 shows the graphical representation of maximum input signal w.r.t. maximum input of zero order INA for the cascaded INA. The maximum input level is decreased by 430dB. The gain for the fifth order of the cascaded INA is approximately 3.2×10^{24} and the maximum input voltage for saturation level of output is $4.686 \times 10^{-24}V$ i.e. a Yokto ($10^{-24}V$) level INA.

PRACTICAL CASCADED INSTRUMENTATION AMPLIFIER & THEIR SIMULATION

Cascaded INA has better amplification for low level signal, the problem arises is high offset voltage [1].

TABLE III. OUTPUT PARAMETERS OF CASCADED INA

S.N.	Parameter	Cascaded INA (Standard Structure)	Cascaded INA (Modified Structure)
1.	V(p-p)	2.78V	5.65V
2.	V(rms)	16.2V	2.02V
3.	V(dc)	16.2V	300mV
4.	V(pp) - Input	2.83nV	2.83nV
5.	Gain	0.9823321×10^9	1.996467×10^9

The circuit diagram of cascaded INA is shown in Figure 7, their simulation shown in Figure 8 and their output parameters are given in Table III. The value of offset DC voltage level goes so high that it becomes practically of no use to simulate cascaded INA. The way out of this problem is to employ a technique which reduces this offset effect to a large extent. Here, we worked on the modified cascaded INA circuit and observed that by the addition of a series capacitor in DA as a blocking capacitor with resistance (R_1). The circuit of modified cascaded INA is shown in Figure 9, their simulation shown in Figure 10 and their output parameters are given in Table III. We can significantly reduce the problem of DC offset voltage. The DC offset voltages reduces from 16.2V to 300mV and gain is approximately double of the modified cascaded INA structure. Similarly, gain is also increases and DC offset voltage is decreases for higher order cascaded INA.

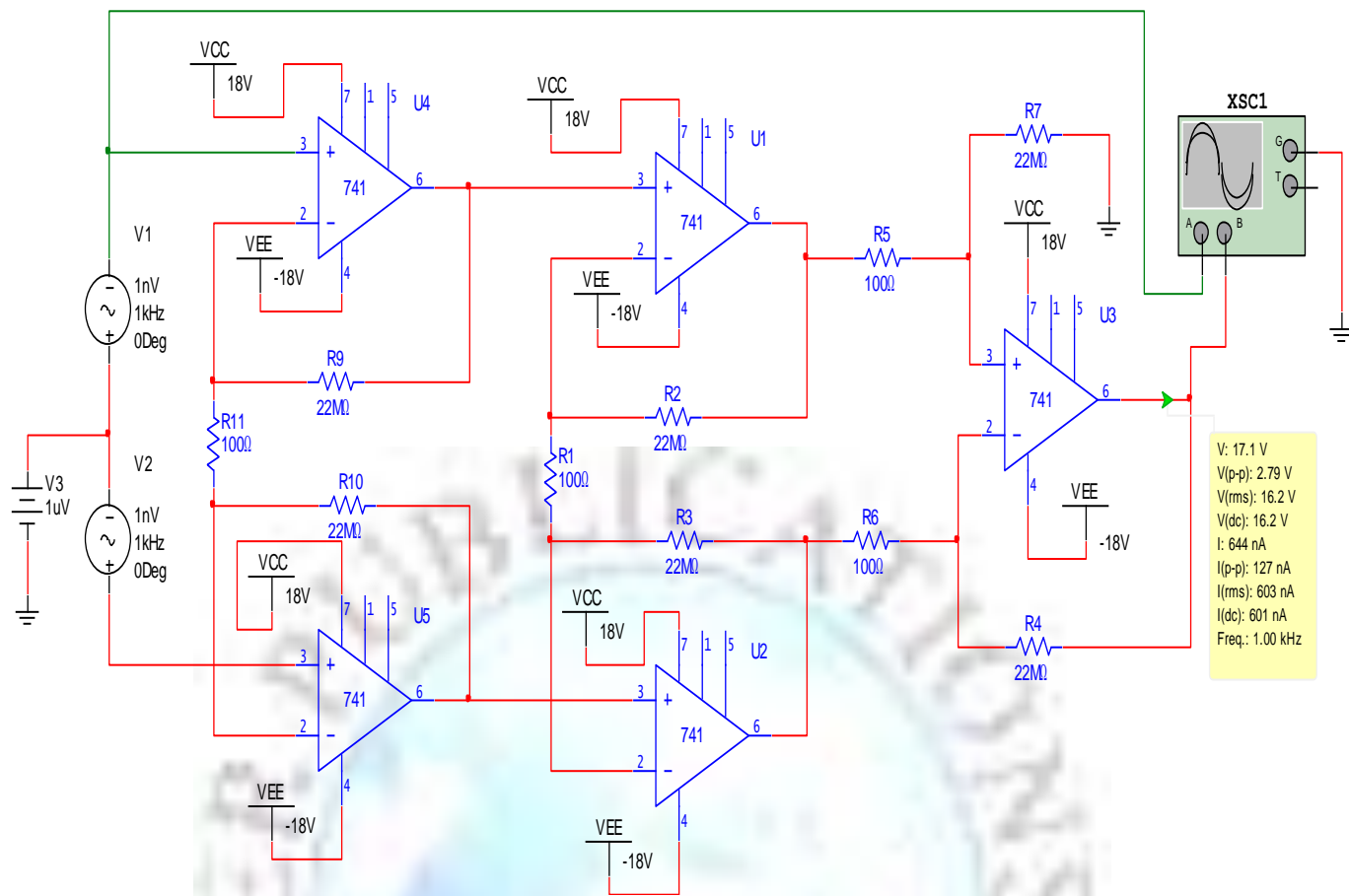


Figure 7. Standard Structure of Cascaded INA on Multisim.

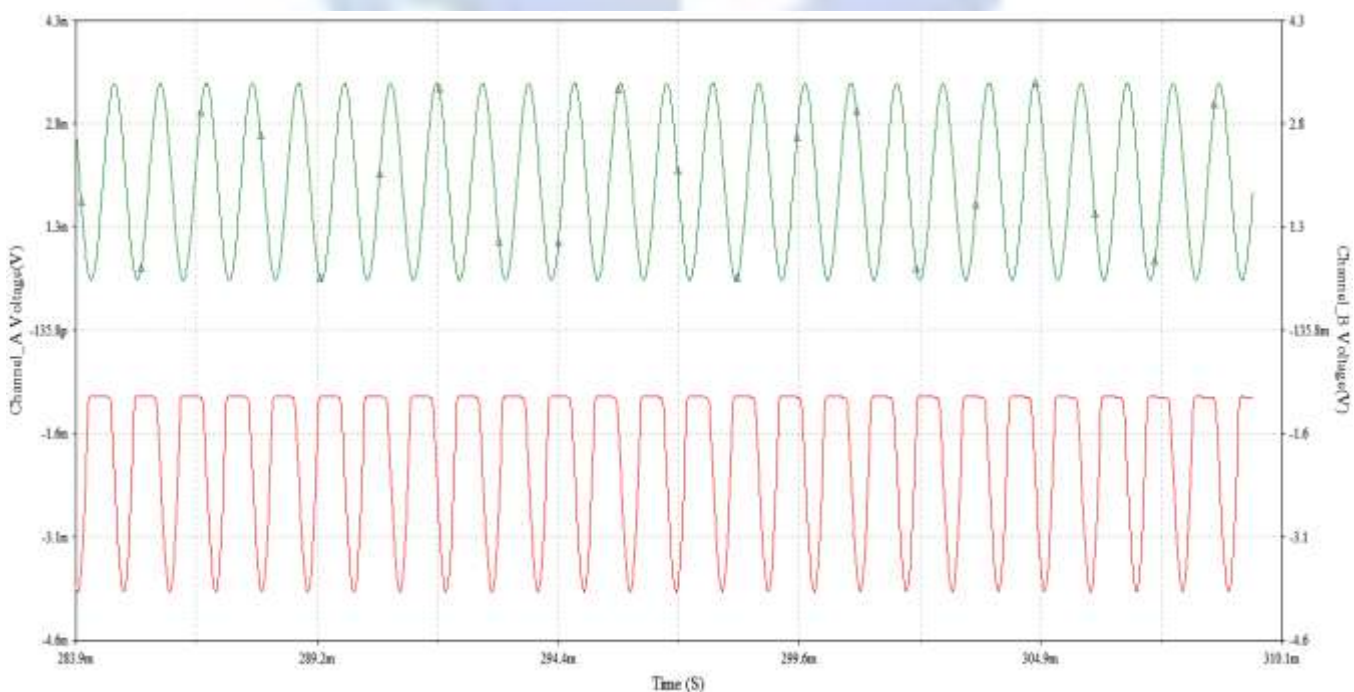


Figure 8. Simulation Results for the Standard Structure of Cascaded INA.

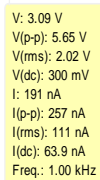


Figure 9. Modified Structure of Cascaded INA on Multisim.

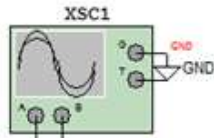
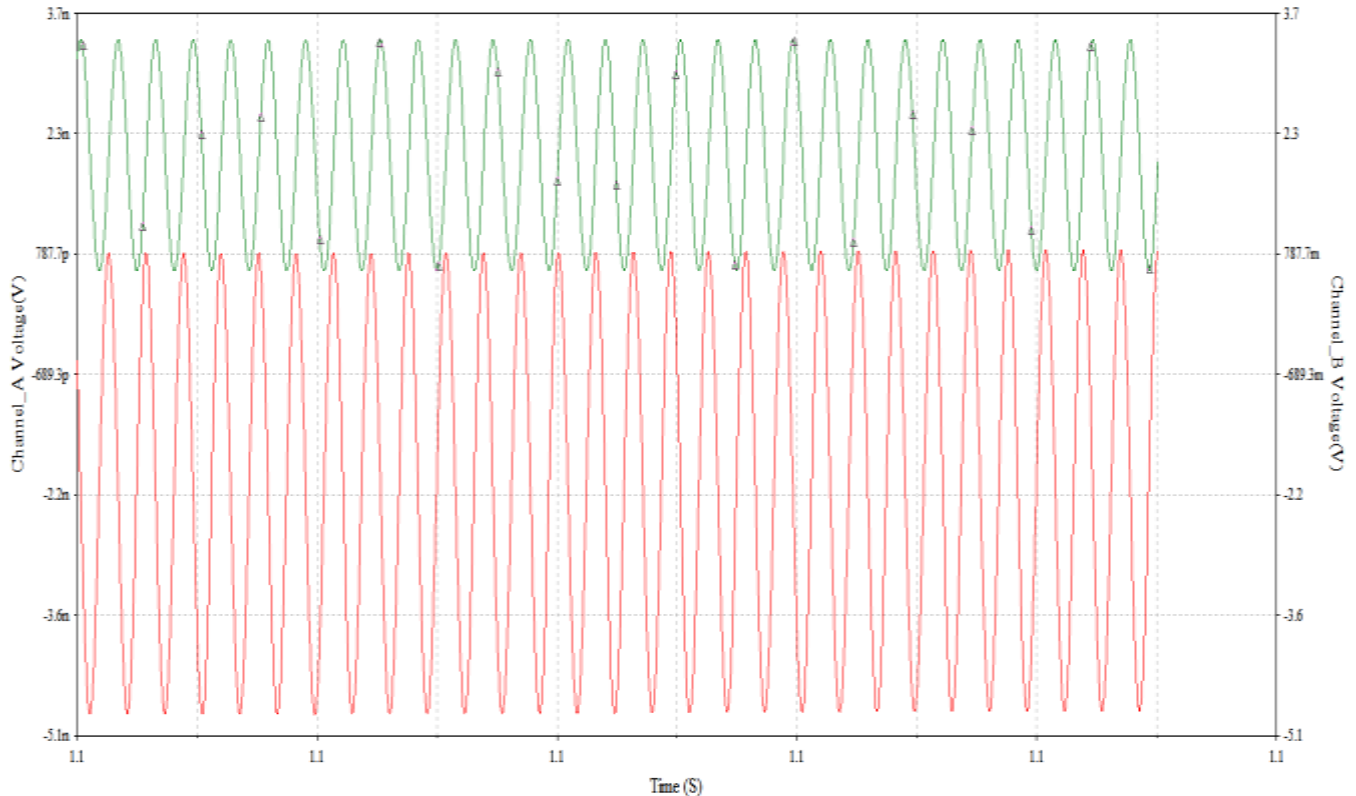


Figure 10. Modified Structure of Cascaded INA



Simulation Results for the Modified Structure of Cascaded INA.

CMOS IMPLIMENTATION OF CASCADED INA WITH DC-OFFSET REDUCTION

A simple two-stage CMOS op amp is used. This circuit configuration provides good common mode range, output swing, voltage gain, stability and bandwidth. Other available topologies are the ones that employ cascode configurations. As the supply voltage is limited, these topologies exhibit inferior input common mode range and output swing. Also, the noise performance is degraded due to more devices in the circuit. The first stage of the op-amp consists of a differential pair with active load. This differential gain stage consists of transistors Q1 through Q4. The amplifier input stage is implemented with PMOS transistors Q1 and Q2. PMOS devices are used as the inputs to the differential pair because of their better noise performance over NMOS transistors; $1/f$ noise is reduced. Also, PMOS input transistors tend to raise unity gain frequency. The non inverting input is the gate of Q2 and the inverting input is the gate of Q1. The differential stage amplifies an applied differential input. G_m of Q2 multiplied by the output resistance at Q2's drain is the gain of this stage.

The current mirror active load is implemented with NMOS transistors Q3 and Q4. These active load devices convert the input signal from a differential signal to a single-ended signal. In other words, the differential output voltage is combined by the current mirror of M3 and M4 resulting in a single output voltage. NMOS transistors are used for this current mirror because we want it to operate fast.

The second stage is another gain stage implemented in a common source configuration with NMOS transistor Q6. Q6 amplifies the single-ended signal at the drain of Q2. PMOS transistor Q7 is the load resistance for Q6; Q7 is this amplifiers current source load. G_m of Q6 multiplied by the output resistance at Q6's drain is the gain of this stage.

PMOS transistor Q8 serves as the current mirror which biases the op-amp by mirroring its current to PMOS transistors Q5 and Q7. The W/L of Q5 and Q7 can be scaled with respect to the W/L of Q8 in order to scale the mirrored current.

Now this single working unit of CMOS implemented Op-Amp is placed instead of typical Op-Amp in figure. 9 to obtain the given CMOS implemented complete figure.10. We keep all the other components value same as that in figure .9 with very little variations as per the requirement of CMOS. In further part of our research we find that in the contemporary world, we need the miniature MOSFET. The researchers are continuously going on for this purpose. The navel of the microprocessor

is latches and again the bare bones of the latches are the MOSFET. Latches are the memory storing cells made up of the logics and upshot of all is the Metal Oxide Field Effect Transistor. If we need to abridge the size of the microprocessor, we will have to allay the size of latches then undoubtedly MOSFET. It is very much clear that as per the size of MOSFET decreases, directly affect the current technology. Now in recent microprocessors, more than 2 billion MOSFETs are in use. So abating the area of that much MOSFETs causes several problems, like switching [2], SCE and DIBL. If we create them in petite way then switching condition will become worst. The double gate (DG) MOSFETs are electro-statically unhelped for others than a single gate MOSFET and empower for supplementary gate length scaling, nanotechnology has accomplished a enormous giant step in fabrication of divergent devices at nanometer like molecular diodes and Carbon Nanotube field effect transistors (CNFETs). Use of DG-MOSFET provided revolutionary scope for VLSI circuits to pull off continues cost cutback and pyrotechnics upswing in post-silicon-based-CMOS-technology. Carbon Nanotube based FET devices are getting fourfold emphasis today due to enhanced I-V characteristics and high channel mobility are perceptive standby for morrow semiconductor devices.

III. CONCLUSION

Many research works are present in the field of electronics as operational and INA but it is the strong effort in this field. The implementation of ideal cascaded INA and used for the amplification of very low i.e. Yokto (10^{-24} V) level signals [1]. Therefore, it can be easily amplify very low level signals and used in many applications like medical instruments, data acquisition systems, physical quantity measuring instruments, etc. But, the practical cascaded INA does not produce the gain upto ideal cascaded INA due to DC offset voltage of op-amp.

In Figure 7, we implement the two stage cascaded INA but gets the high DC offset voltage i.e. approximately 16.2V but the AC signal voltage (pp) is 2.78V only. If we passes this signal on next stage we only received the +ve saturation value. So, it can't work for more than more than two stages and AC output signal is also clipped for two stages cascaded INA. Therefore, In this paper, we presents the modified cascaded INA which reduces the DC offset output voltage with high range and gives the better result in comparison of standard cascaded INA. The DC offset output voltage is 300mV for modified cascaded INA. Their offset value is approximately reduces upto 50 times from their ideal structure. So, we can use more than two stage of cascaded INA. Here, the modified cascaded INA introduces a blocking capacitor for the reduction of DC offset voltage.

The problem which comes in the way is, with every step of cascading the size of the circuit increases and so the power requirements. In this paper we deal with this problem and find that we can reduce the size of the circuit considerably by replacing traditional op-amp with two stage CMOS op-amp. Use of DG-MOSFET provided revolutionary scope for VLSI circuits to pull off continues cost cutback and pyrotechnics upswing in post-silicon-based-CMOS-technology. Carbon Nanotube based FET devices are getting fourfold emphasis today due to enhanced I-V characteristics and high channel mobility are perceptive standby for morrow semiconductor devices.

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