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The Novel Design of Cascade Multilevel Inverter Topology for Solar PV System S. Karthik¹, Dr. J. kanakaraj²

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Abstract: Multilevel voltage source inverter offer several advantages compared to their conventional counterparts. Cascaded H-bridge inverter provides Stepped AC voltage wave form with lesser harmonics at higher levels by combining different ranges of voltage DC sources and the filter components are reduced by increasing Step levels. By increasing the level of the inverter we can get several advantages: get a good voltage wave form, Very low THD, reduced volume and cost. The need of several sources on the DC side of the converter makes multilevel technology attractive for photovoltaic applications. This paper provides an overview of a multilevel inverter topology and investigates their suitability for single-phase photovoltaic systems. A simulation model is based on MATLAB/SIMULINK is developed. An experimental 40W prototype inverter was built and tested. The results is experimentally validate for the proposed SPWM based three H-bridge 27 level cascaded multilevel inverter.

Keywords: Cascaded H-bridge multilevel inverter, Dc link voltage.

I. INTRODUCTION

Cascaded multilevel inverter topology is based on the Stepped AC voltage wave form with lesser harmonics at higher levels by combining different ranges of DC voltage sources [2]. By increasing the number of DC voltage Sources at different ranges, the stepped sinusoidal output waveform adds more steps. Multilevel inverters are used in high power applications such as Hybrid System, Solar system, and Flexible AC transmission systems [1][3]. Due to the need of filters is reduced by increasing the voltage level and the efficiency is high because of lesser harmonic. In low power applications where switching frequencies are not as restricted as in high power applications various control methods such as multicarrier pulse width modulation or multiple hysteresis band control methods can be used to further reduce harmonics in the stepped waveforms. Cascaded Multilevel inverter is suitable for solar PV systems due to their cell structure. Each solar array provides different DC voltage levels. A multilevel converter not only achieves low power ratings, but also enables the use of renewable energy sources. In high power applications we can easily interface the Cascaded H-Bridge inverter with Solar PV module and fuel cells [4], [5].

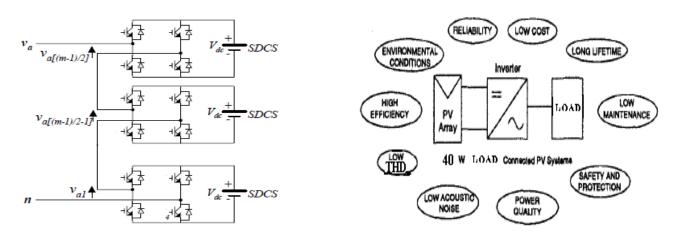


Fig.1 Single-Phase structure of a multilevel H-bridges inverter

Fig.2 Advantages of 27-level multilevel H-bridges inverter

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Cascaded inverter has high DC link voltage and the DC link Voltage also has a less switching frequency and it reduces the switching loss. They allow to combine different types of switches to optimize the inverter efficiency. The new hybrid multilevel inverter consists of full bridge modules which have the relationship of 1v, 3v, 9v.....3s-1v for DC link Voltage .The output waveform has 27 levels, \pm 13, \pm 12, \pm 11, \pm 10, \pm 9, \pm 8, \pm 7, \pm 6, \pm 5, \pm 4, \pm 3, \pm 2, \pm 1, 0.

The inverter generates 3s different voltage levels (e.g. An inverter with s=3 cells can generate 33=27 different voltage level). The basic hybrid multilevel inverter structure for single phase is illustrated in Fig.1.This multilevel inverter is made up of a set of series connected cells. Each cell consists of a 4-switch H-bridge voltage source inverter. The output inverter voltage is obtained by summing the cell contributions. In conventional method, low level inverters are used. Better sinusoidal output was not obtained which is the drawback of the conventional system and the harmonics was high. By increasing the number of steps in the Cascaded H-bridge inverter, we can get a high efficiency with lesser harmonics and good resolution and good stepped voltage wave form [6].

Cascaded H-bridge inverter is developed by connecting more number of single stage inverter with different voltage sources in series. The common function of multilevel inverter is to synthesize a desired voltage from several separate DC sources. Each inverter is capable of generating three different output voltages, +Vdc, 0 and - Vdc [7].

II. MODELING OF MULTILEVEL NEW HYBRID INVERTER

For each full bridge inverter the output voltage is given by

$$\mathbf{V}_{Oi} = \mathbf{V}_{dc} \ (\mathbf{S}_{1i} - \mathbf{S}_{2i})$$

and the input DC current is,

 $I_{dci} = I_a (S_{1i} - S_{2i})$

i = 1,2,3...(number of full bridge inverters employed). I_a is the output current of the new hybrid inverter. S_{1i} and S_{2i} is the upper switch of each full bridge inverter. A single phase output voltage of proposed inverter is given by

$$V_{on} = \sum_{i=1}^{n} V_{0i}$$

III. 27- STAGE MULTILEVEL INVERTER PROPOSED TOPOLOGY

The topology of the proposed DC–AC H-bridge multilevel inverter is shown in Fig.3. The inverter uses a standard three-leg and an H-bridge with its DC source in series with each phase leg.

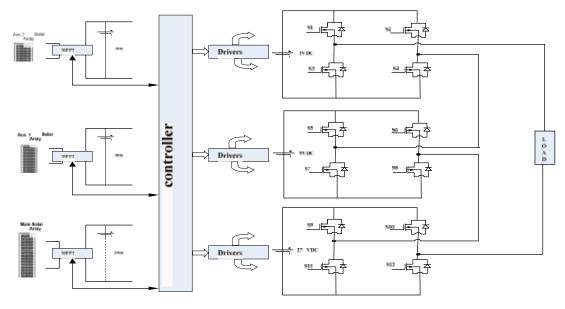


Fig.3 Single phase proposed DC-AC three H - bridge 27 level multilevel inverter



VOL. 2 ISSUE 2, FEB.-2013

ISSN NO: 2319-7463

In this cascaded H-bridge inverter, it has three voltage sources as an input to the three H-Bridges and all the three H - bridges are connected in series like in the proposed method of the inverter. Each H-bridge has a Semiconductor switches like IGBT or MOSFET or any other semiconductor devices. In this proposed model four MOSFET switch is used for each H-bridge. In this H-bridge the two semiconductors are switched for one half cycles either positive or negative. The switching for one positive cycle is as S1, S4 and S5, S8 and S9, S12 this method is adopted to protect the circuit from short circuiting and by connecting the number of modules in series we can increase the level of the inverter to obtain sinusoidal waveform.

IV. WORKING PRINCIPLE OF THREE H- BRIDGE 27-LEVEL INVERTER

The topology of the proposed DC–AC H-bridge multilevel inverter is shown in Fig.4. The inverter uses a standard three-leg inverter and an H-bridge with its DC source in series with each phase leg. To see how the system operates, consider simplified single phase topology, shown in Fig.4. The output voltage v1 (3v) of this first leg of the top inverter is goes to ON state. For a negative half cycle this leg is connected in series with a full H-bridge, which, in turn, is supplied by a supply voltage. If the supply is kept charged to Vdc/2, then the output voltage of the H-bridge can take on the values +Vdc/2 (S2,a1) and Vdc/2 (S2,a4 & S2,b1 & S2,b4 & S2,c4).

	Output voltages and switching states for the new hybrid inverter ,S=3																										
	Vout																										
Vdc	- 13V	- 12V	- 11V	- 10V	- 9V	- 8V	- 7V	- 6V	- 5V	- 4V	- 3V	- 2V	1V	0V	1V	2V	3V	4V	5V	6V	7V	8V	9V	10V	11V	12V	13V
1v	N	0	Ρ	Ν	0	Ρ	N	0	Р	Ν	0	Р	z	0	Р	Ν	0	Р	N	0	Р	Ν	0	Ρ	Ν	0	Ρ
3v	N	Ν	Ν	0	0	0	Ρ	Р	Р	Ν	Ν	Ν	0	0	0	Р	Р	Р	N	Ν	Ν	0	0	0	Р	Ρ	Р
9v	N	Ν	N	Ν	Ν	Ν	Ν	Ν	Ν	0	0	0	0	0	0	0	0	0	Ρ	Ρ	Ρ	Ρ	Ρ	Ρ	Ρ	Ρ	Р

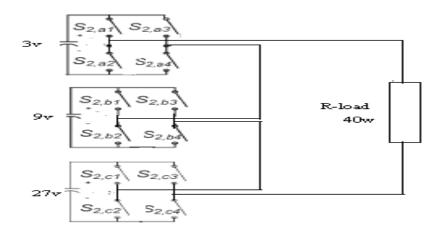


Fig.4 Working principle of Single phase of the proposed DC-AC three H-bridge using [27-level] multilevel inverter.

When the output voltage v = v1 + v2 + v3 is required to be zero, one can either set

v1 = +Vdc/2 and v2 = +Vdc/2 and v3 = -Vdc/2 (or)

v1 = -Vdc/2 and v2 = +Vdc/2 and v3 = +Vdc/2

V. CONDUCTION SWITCH STATE FOR 180° MODE OF OPERATION

The mentioned below table shows the Conduction mode of the switches for 180°.



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VOL. 2 ISSUE 2, FEB.-2013

	1		
S.No.	Switching pattern	Switching pattern	Output
	for first 90° modeof	for first 90° mode	Voltage
	operation	of operation	(V_o)
1	\$1,\$4,\$5,\$6,\$9,\$10	\$1,\$4,\$5,\$8,\$9,\$12	3V
2	\$2,\$3,\$5,\$8,\$9,\$10	\$1,\$2,\$5,\$8,\$9,\$12	6V
3	\$1,\$2,\$5,\$8,\$9,\$10	\$2,\$3,\$5,\$8,\$9,\$12	9V
4	\$1,\$4,\$5,\$8,\$9,\$10	\$1,\$4,\$5,\$6,\$9,\$12	12V
5	\$2,\$3,\$6,\$7,\$9,\$12	\$1,\$2,\$5,\$6,\$9,\$12	15V
6	\$1,\$2,\$6,\$7,\$9,\$12	\$2,\$3,\$5,\$6,\$9,\$12	18V
7	\$1,\$4,\$6,\$7,\$9,\$12	\$1,\$4,\$6,\$7,\$9,\$12	21V
8	\$2,\$3,\$5,\$6,\$9,\$12	\$1,\$2,\$6,\$7,\$9,\$12	24V
9	\$1,\$2,\$5,\$6,\$9,\$12	\$2,\$3,\$6,\$7,\$9,\$12	27V
10	\$1,\$4,\$5,\$6,\$9,\$12	\$1,\$4,\$5,\$8,\$9,\$10	30V
11	\$2,\$3,\$5,\$8,\$9,\$12	\$1,\$2,\$5,\$8,\$9,\$10	31V
12	\$1,\$2,\$5,\$8,\$9,\$12	\$2,\$3,\$5,\$8,\$9,\$10	33V
13	\$1,\$4,\$5,\$8,\$9,\$12	\$1,\$4,\$5,\$6,\$9,\$10	39V

VI. SWITCHING TECHNIC OF THREE H-BRIDGE MULTILEVEL [27 LEVEL] INVERTER

There are several kinds of modulation control methods such as traditional pulse width modulation (SPWM), space vector PWM, harmonic optimization or selective harmonic elimination, and active harmonic elimination, and they all can be used for inverter modulation control. In this proposed system sinusoidal pulse width modulation (SPWM) switching scheme is used to provide firing pulse to on and off the semiconductor switch at desired switching frequency. The Fourier series expansion of the fundamental frequency (staircase) output voltage waveform of the multilevel inverter, as shown in Fig.6.

$$V(\omega t) = \frac{4V}{\pi 2} \times \sum_{n=1,3,k_{\rm out}} \frac{1}{n} \left(\cos(n\theta_1) + \cos(n\theta_2) \right) \sin(n\omega t) \,.$$

The key issue of fundamental frequency modulation control is choice of the two switching angles θ_1 and θ_2 . The given mathematical equation is used to eliminate the fifteenth order harmonics.

(i)

(v)

$$m_{a} = \cos (\theta_{i}) + \cos (\theta_{ii})$$

$$0 = \cos (15\theta_{i}) + \cos (15\theta_{ii})$$
 (ii)

 m_a = Modulation index of the output voltage.

 $\theta_{i}, \theta_{ii} = Unknown parameters.$

Modulation index is defined as

$$m = \frac{V_1}{V_{def/2}}$$
(iii)

The relationship between the output voltage index ma and modulation index m is

$$m = \frac{4}{\pi}m_{\alpha} \tag{iv}$$

Modulation index for a SPWM based multilevel inverter is m=1 for without third order harmonic compensation m=1.5 for with third order harmonic compensation

Cascaded H-bridge multilevel inverter output voltage waveform is a Stepped sinusoidal waveform, not a square waveform. The maximum modulation index for linear operation m is 2.42. Amplitude modulation index for an n-level inverter

$$m_a = \frac{A_m}{(m-1)A_C}$$



(vi)

VOL. 2 ISSUE 2, FEB.-2013

where,

 A_m - Peak to Peak reference waveform amplitude.

Ac - Peak to Peak Carrier waveform.

VII. HARMONIC ELIMINATION IN MULTILEVEL INVERTER

The output voltage V(t) of the multilevel inverter can be expressed in Fourier series as

$$V(t) = \sum_{n=1}^{\infty} (a_n \sin n\alpha_n + b_n \cos n\alpha_n)$$

Due to quarter wave symmetry of the output voltage the even harmonics are absent ($b_n=0$) and only odd harmonics are present. The amplitude of the n^{th} harmonic a_n is expressed only with the first quadrant switching angle $\alpha_1, \alpha_2, \dots, \alpha_m$.

$$a_{n} = \frac{4 \operatorname{V}_{do}}{n \pi} \sum_{k=1}^{n} (\cos n \alpha_{n})$$

$$\theta < \alpha_{1}$$
(vii)

For any odd harmonics can be expressed up to k^{th} term, where m is the number of variable corresponding to switching angle α_1 through α_m of the first quadrant

Total Harmonics Distortion (THD):

$$THD = \frac{1}{fundamental} \sum_{n=2}^{\infty} (n^{th} harmonic \, components)^2 * 0.5$$

VIII. INVERTER EFFICIENCY

Cascaded hybrid inverter efficiency is higher for the applications where the switching losses are bigger than a conventional inverter and the selection of voltage sources are given below for a corresponding topology and number of stages.

Topology	Voltage Sources	No. of stages
Cascaded	V _{dc}	2n+1 for
	1V _{dc}	7-level, where n=3
Hybrid	$2^{n-1} V_{dc}$	2^{n+1} -1 for
	4 V _{dc}	15-level
Proposed	$3^{n-1} V_{dc}$	3 ⁿ
Hybrid	9 V _{dc}	27-level

IX. SIMULATION RESULTS

In general there are two modulation control schemes, it will be used for multilevel inverter they are fundamental switching frequency and high switching frequency Pulse Width Modulation. In this proposed paper, the simulation model based on the MATALB/SIMULINK and the model is developed under the high switching frequency SPWM. It has triangle carrier signal, one carrier signal for each level and it has one reference or modulation, signal for a single phase.

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VOL. 2 ISSUE 2, FEB.-2013

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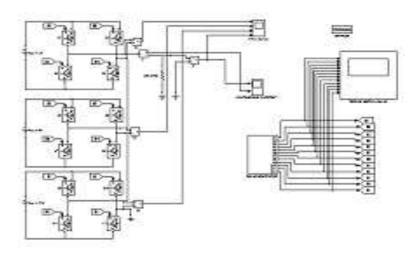


Fig.5 The above figure shows the overall block diagram of 27-level multilevel inverter

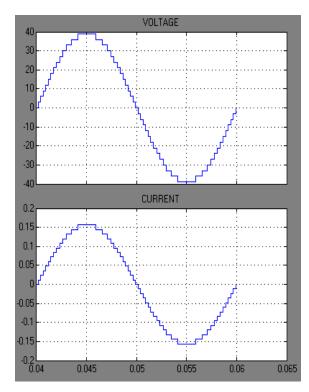


Fig. 6 Output voltage and Output current waveforms

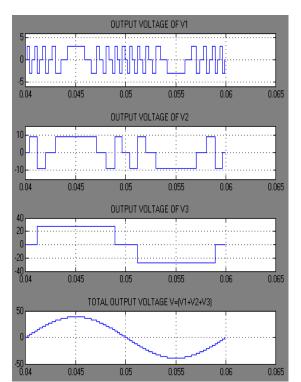


Fig.7 Output voltage regulation for all the three H-bridges and total output voltage (v=v1+v2+v3)

X. RESULT OF TOTAL HARMONICS DISTORTION

The Total Harmonic Distortion of a 27 - level multilevel inverter was analyzed by Fast Fourier Transformation method (FFT) for three cycles and the low order harmonics are eliminated up to 13^{th} order and the result of FFT method is shown in below diagram. THD of the proposed inverter is 3.04%.



VOL. 2 ISSUE 2, FEB.-2013

ISSN NO: 2319-7463

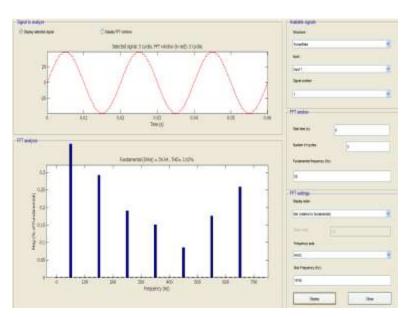


Fig. 8 Total Harmonic distortion for 27-level inverter

XI. CONCLUSION

In conventional method, low level inverter is used for solar PV applications, sinusoidal output was not obtained which is the drawback of the conventional system and the harmonics was 30%. In proposed system the level of the inverter was increased and hence the output waveform is sinusoidal.

The multilevel inverter has introduced a solution to increase the inverter output voltage above the voltage limits of classical semiconductors. There are quite a lot of ways to achieve multilevel inverters. The most important topologies are the neutral point clamped inverters, the flying capacitors and the cascade inverters. This project investigates new hybrid twenty seven level multilevel inverter for solar PV applications, which significantly increase the number of levels in output voltage waveform and thereby dramatically reduces the

low order harmonics of 3rd, 5th, Upto 13th and Total Harmonics Distortion of 3.04%. Moreover the stage with higher DC link voltage has less switching frequency and therefore reduced switching losses.



Fig.9 Overall system of the project





VOL. 2 ISSUE 2, FEB.-2013

ISSN NO: 2319-7463

The new hybrid multilevel inverter consists of three full bridge modules, each module has four MOSFET switches IRFZ44, which have the relationship of 3V, 9V and 27V for DC link Voltage or solar panel input and the output voltage is 39V. The scaling of voltages for each module is in the power of three.

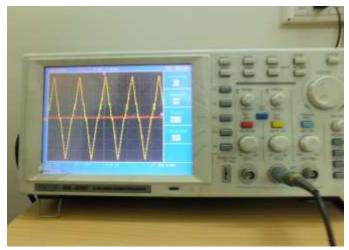


Fig.10 Output of a 27-Level Multilevel inverter

Future Works

This project can be extended up to 81-Levels by using four DC sources and sixteen semiconductor switches. Due to increasing level, the filtering components are reduced.

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