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Pipeline ADC using Switched Capacitor Sharing Technique with 2.5 V, 10-bit

Ankit Jain
Dept. of Electronics and Communication, Indore Institute of Science & Technology, Indore, India

Abstract: This paper presents 10-bit, 1.5 MS/s, 2.5V, Low Power Pipeline analog to digital converter using capacitor coupling techniques. A capacitance coupling folded-cascade amplifier effectively saves the power consumption of gain stages of ADC in a 0.25 µm CMOS technology. The ADC also achieves Low power Consumption by the sharing an op-amp between two successive pipeline stage further reduction of power is achieved by removing front end SH circuit from third stage onwards. The ADC, implemented in a 0.25 µm CMOS technology, achieves 10-bit resolution and consumes 13.3 mW power at 5 MHz sampling frequency.

Index terms: Analog to Digital conversion, capacitor sharing, high speed OPAMP-sharing pipelined analog to digital convertor, Low power.

1. INTRODUCTION

Most of the natural signals are analog in nature and sensors that sense the nonelectrical quantities are also in analog nature. Today most of the electronic systems works on digital domain because of their accuracy and reliability, so in order to sense and process the analog signals and connect with digital systems there is requirement of an analog to digital converter.

Pipeline ADC architecture is widely used in applications requiring high speed and high resolution with relatively low power dissipation. For low power dissipation various technique are used, switch capacitor technique is one of them. This technique enable to reduce the total static power dissipation [1]-[4].

This paper proposes to use switch capacitor technique and capacitor coupling technique in 0.25µm CMOS technology at 2.5 V. Further power dissipation is reduced by removing load capacitance and using feedback capacitor as load capacitor.

The outline of this paper is as follows, 2. ADC Architecture, 3.Design of building blocks, 4.Simulated results and 5.Conclusion.

2. ADC ARCHITECTURE

The pipelined ADC is made of cascaded similarly structured stages separated by S/Hs. Each pipelined stage generates a coarse ADC output and a reconstructed residue signal for the later stages. The S/H enables the concurrent operation of the pipelined stages for a high throughput rate. The capacitor-array MDAC performs all of the above functions except for that of the coarse ADC. Assume that N_i bits have to be resolved in the i^{th} pipelined stage. The output residue V_{RESi} is generated after the coarse ADC generates an N_i -bit digital code. The residue is defined as the unquantized portion of the signal obtained by subtracting the output of the reconstruction DAC from the signal [2]. The residue is amplified by 2^{Ni}-2 , which is half of the ideal gain. This allows the other half of the range to be used for digital error correction. The full signal range is divided into 2^{Ni}-1 ranges using 2^{Ni}-2 comparators. In general,the residue output V_{RES} of a stage expressed in terms ofthe stage resolution n is

$$V_{RES} = 2^{n-1} V_{IN} - bV_{REF}$$

Where $b = \pm(2^{k-1} - 1)$, and k = 1,……, n, depending on the coarse ADC result. This residue output is further quantized in finer steps by the later stages in the pipeline.

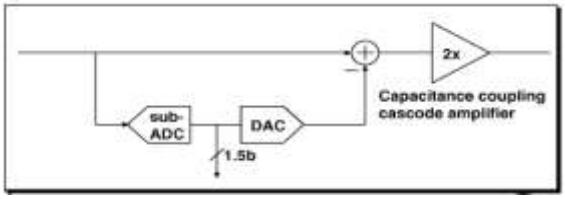

Fig1. A Pipeline ADC architecture.

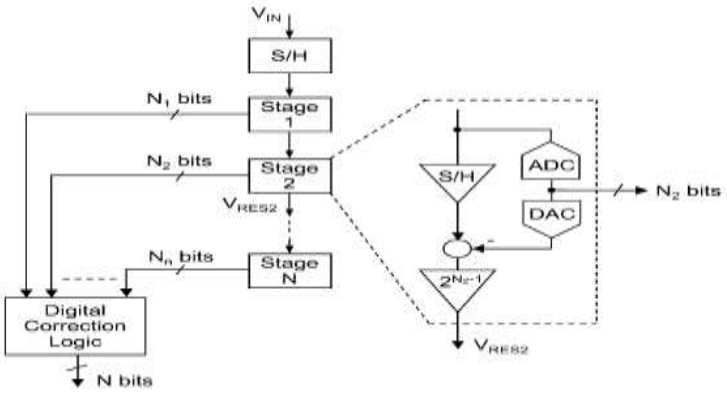

Fig 2: N-bit pipeline ADC architecture

In this paper 10 bit is implemented by using 1.5 bit sub ADC because of its speed and its accuracy. 10 bit is implemented in nine stages, eight stages of 1.5 bits and ninth stage of 2 bit sub ADC. Sample and hold is attached with the first stage but from second stage on words S/H is removed to save power, by doing so it is possible to have some error in the MDAC output but for 10 bit or less this error is acceptable and does not affect the overall response.

3. DESIGN OF BUILDING BLOCKS

A. Sample and Hold

An important application of the switch is in the sample and hold circuit. The sample and hold circuit finds extensive use in data converter application as a sampling gate. A variety of topologies exist, each with their own benefits. The simplest is shown in Fig.3 A clock plus applied to the gate of Transmission gate, enable V_{in} to charge the hold capacitor, C_H. The width of the strobing gate pulse should allow the capacitor to fully charge before being removed. The Op-amp simply acts as unity gate buffer isolation the hold capacitor from any external load [5].

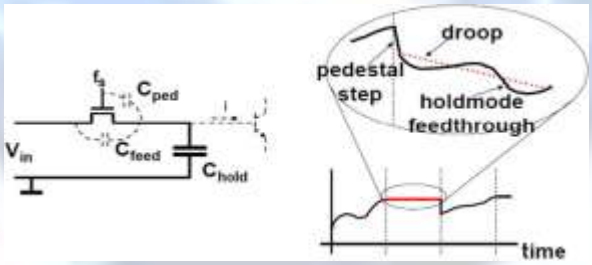

Fig 3: Sample and Hold

B. Comparator

Comparator is very important building block of any ADC architecture. Comparator implemented in this paper can be divided into three parts, Preamplification stage, Decision circuit (positive feedback) and Postamplification (output buffer) [5]-[6].

Preamplification

This circuit is a differential amplifier with active loads. The transconductance, $g_m$sets the gain of the stage, while the input capacitance of comparator is determined by the sizes of M1 and M2. The input voltages and output current is related by

$$i_{op} = \frac{g_m}{2}(v_p - v_n) + \frac{I_{ss}}{2} = I_{SS} - i_{om}$$

If $v_p > v_m$, then $i_{op}$is positive i_{on} is negative ($i_{op} = -i_{on}$)

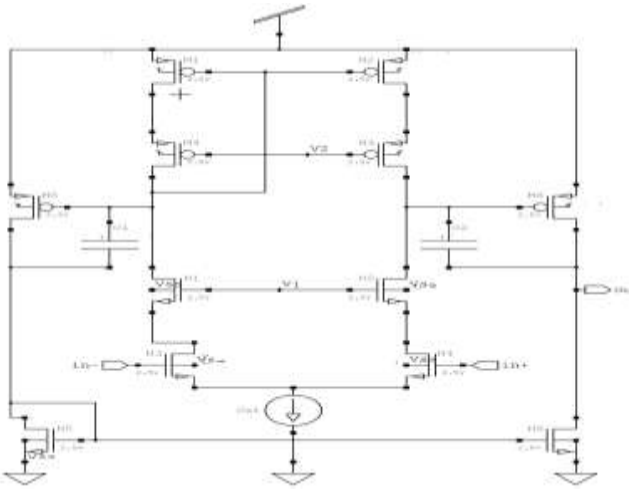

Fig 4: Comparator Circuit

Decision Circuit

Decision circuit uses positive feedback from the cross-gate connection of M6 and M7 to increase the gain of the decision element. If $i_{op} >> i_{on}$ then v_{on} is approximately 0 V and v_{op} is

$$v_{op} = \sqrt{\frac{2i_{op}}{\beta_A}} + V_{THN}$$

Output Buffer

The final stage is output buffer is to convert the output of the decision circuit into a logic signal (i.e, 0 or VDD). The output buffer should accept a differential input signal and not have slew-rate limitations.

C. Opamp Circuit

The Opamp circuit used in this paper is shown in Fig 5. The Opamp architecture is folded- cascode type. Opamp is very important building block in ADC to convert digital signal to analog signal. This opamp is used in MDAC circuit. Second stage is attached with this opamp to increase the gain and the output swing. In this architecture PMOS cascade current mirror is used that gives $V_X = V_{DD} - |V_{GS5}| - |V_{GS7}|$, limiting the maximum value of V_{out} to $V_{DD} - |V_{GS5}| - |V_{GS7}| + |V_{TH6}|$. The PMOS load as shown in opamp is modified so that M7 and M8 are biased at the edge of the triode region [

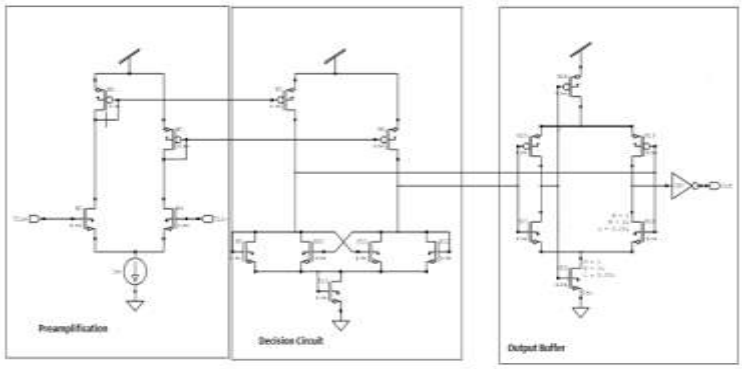

Fig 5.Opamp Circuit

D. MDAC

With switch capacitor circuits it is possible to perform highly accurate mathematical operations such as addition, subtraction, and multiplication (by a constant), due to the availability of capacitors with a high degree of relative matching. Switch capacitor circuits also facilitate multiple, simultaneous signal manipulations with relatively simple architectures. It is possible to combine the functions of sample and hold, subtraction, DAC, and gain into a single switched capacitor circuit, referred to as the Multiplying Digital-to-Analog Converter (MDAC) [1]-[3] as shown in Fig. 6

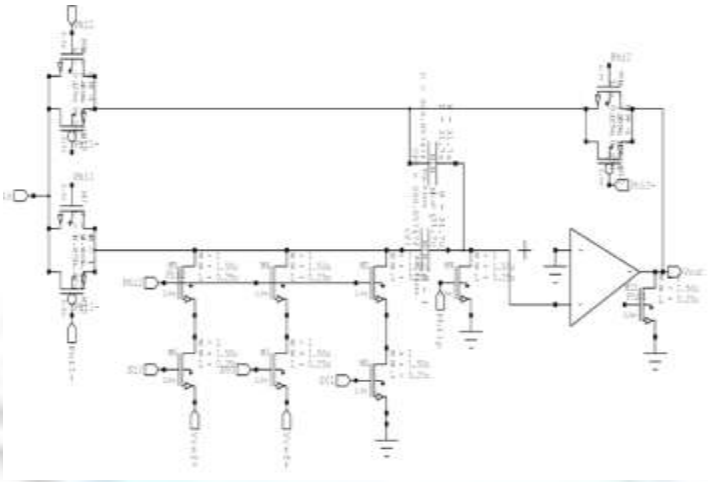

Fig 6. MDAC Circuit

A 1.5 bits/stage architecture has one of three digital outputs, thus the DAC has three operating modes.

ADC output=01: No over rage error (stage input between $-V_{ref}/4$ and $+V_{ref}/4$.

During $\phi 1$: $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$

During $\phi 2$: C1 is discharged, thus by charge conservation: $C_1 V_{in} + C_2 V_{in} = C_2 V_{out}$

Thus $V_{out} = \frac{C_1 + C_2}{C} V_{in} \rightarrow if C_1 = C_2, then: V_{out} = 2V_{in}$

ADC output = 10: Over rage error-Input exceeds $V_{ref}/4$, thus subtract Vref/2 from input

During $\phi 1$: $Q_{C1} = C_1 V_{in}, Q_{C2} = C_2 V_{in}$

During $\phi 2$: C1 is charged to Vref. Thus by charge conservation

C1Vin + C2Vin = C1Vref +C2Vout

$$\therefore V_{out} = \frac{C_1 + C_2}{C_2} Vin - \frac{C_1}{C_2} V_{ref} \rightarrow if C_1 = C_2, then: V_{out} = 2V_{in} - Vref = 2(V_{in} - V_{ref}/2)$$

ADC output = 00: Under range error – Input below -Vref/4, thus addVref/2 to input

During φ1 : QC1=C1Vin, QC2=C2Vin

During φ2 : C1 is charged to -Vref, thus by charge conservation

C1Vin + C2Vin = C1(-Vref)+C2Vout

$$\therefore V_{out} = \frac{C_1 + C_2}{C_2} Vin + \frac{C_1}{C_2} V_{ref} \rightarrow if C_1 = C_2, then: V_{out} = 2V_{in} + Vref = 2(V_{in} + V_{ref}/2)$$

Thus the switched capacitor circuit implements the stage sample-and-hold, stage gain, DAC, and subtraction blocks [4]. Signal dependent charge injection is minimized by using bottom plate sampling, where the use of an advanced clock φ1p, makes charge injection signal independent. A nonoverlapping clock generator is thus required for the MDAC.

4. SIMULATED RESULTS

A. Sample and Hold Response

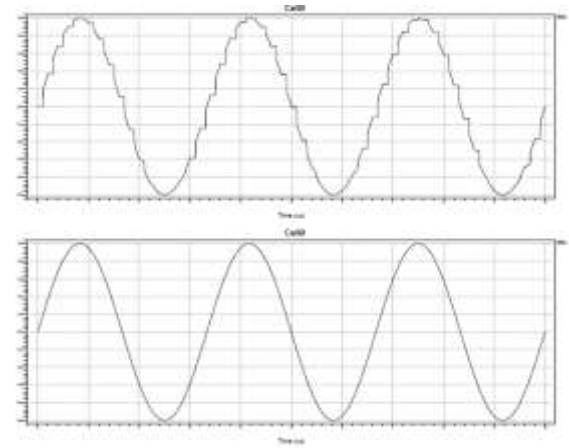

Fig 7: Simulated result of Sample and Hold

B. Comparator

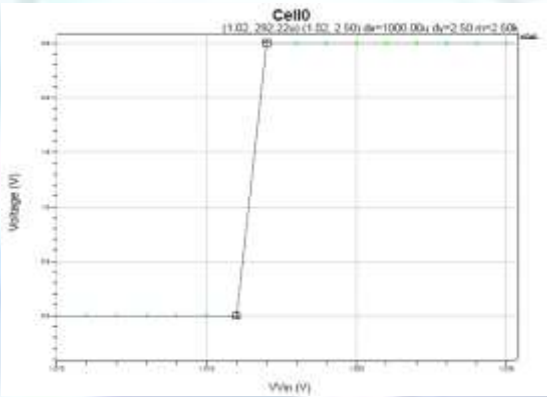

Fig 8. DC Characteristic of Comparator

Comparator DC gain: 2500
UGB : 684.16 MHz

C. Opamp

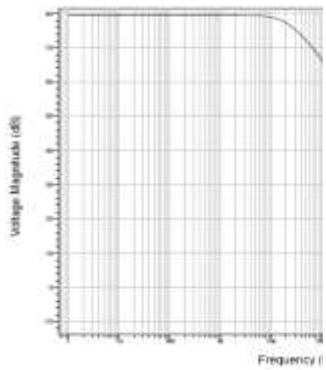

Fig 9. Gain Plot of Op-amp
Gain : 80 dB

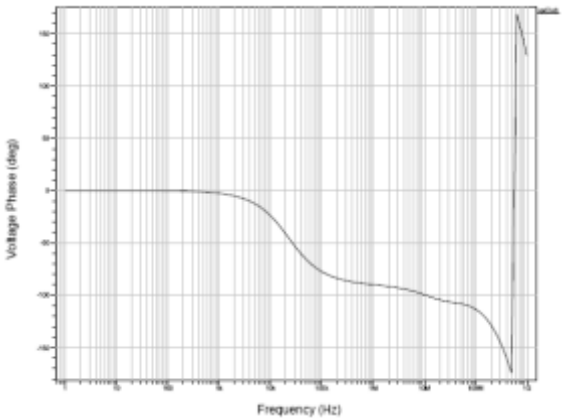

Fig 10. Phase plot of Opamp

Phase Margin : 62.5 dB

D. MDAC

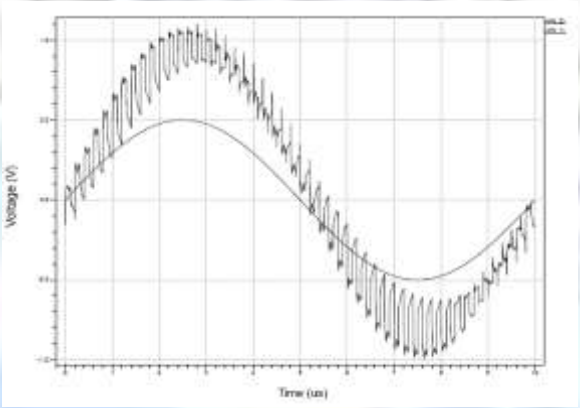

Fig 11. Output of MDAC

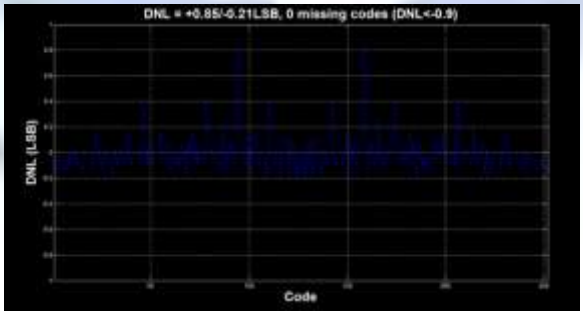

Fig 12. DNL of ADC

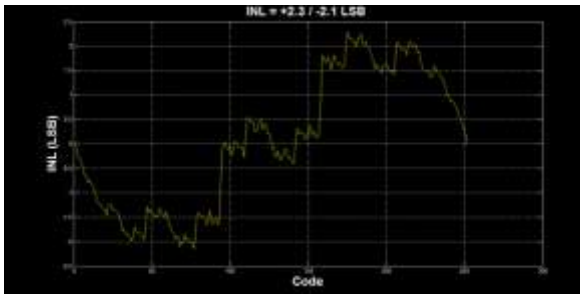

Fig 13. INL of ADC

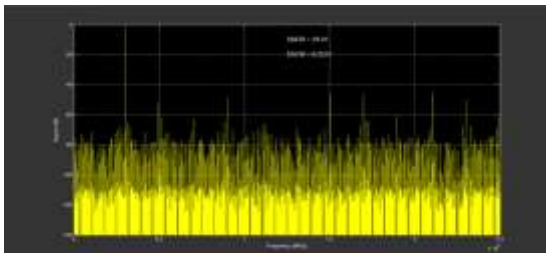

Fig 14. SNDR plot at f=5MHz

Performance Summary

Technology	0.25 µm CMOS process
Resolution	10 bit
Supply Voltage	2.5 V
Conversion rate	5 MS/s
SNDR	39.41 dB
ENOB	6.25
INL/DNL	+2.3/-2.1 LSB/ +0.85/-0.21 LSB
Power	204.9 mW

CONCLUSION

The presented capacitor sharing technique significantly reduces the effective load capacitance, thereby reducing the power consumption of the opamps. Further power consumption is reduced by removing front end S/H circuit that do not affect the response for resolution less than 10 bit.

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