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Topologies and Control strategies of a Multilevel Inverter

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Abstract: Multilevel inverters have been attracting in favor of academia as well as industry in the recent decade for high-power and medium-voltage energy control. In addition, multilevel power inverters can provide more than two levels of voltage to achieve smoother and less distorted dc-to-ac power conversion. The multilevel concept is used to decrease the harmonic content without any change or decrease in the inverter output.In this paper the important topologies of multilevel inverter like diode-clamped inverter (neutral- point clamped), capacitor-clamped (flying capacitor) and cascaded multilevel inverters. In this paper the most important modulation methods developed for these multilevel inverters are presented: multilevel sinusoidal pulse width modulation, selective harmonic elimination, and space-vector control and modulation are shown respectively. Some application examples of these multilevel topologies will be given.

Keywords: Diode Clamped Inverter, Capacitor Clamped Inverter, Cascade H-Bridge Inverter, Modulation Technique.

I. Introduction

Multilevel inverters have been used for dc-to-ac power conversion in high-power applications such as utility and large motor drive applications. Multilevel inverters provide more than two voltage levels. The unique structure of multilevel voltage source inverters allow them to reach high voltages with low harmonics without the use of transformers or series connected synchronized switching devices. The harmonic content of the output voltage waveform decrease significantly.

There are three major multilevel topologies: cascaded, diode clamped, and capacitor clamped [1]. For the number of levels (M) no greater than three (i.e. $M \leq 3$), or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. Infact, each voltage level can be supported by a capacitor and proper control [2]. However, for M >3 and applications involved in active power transfer, such as motor drives, these multilevel converters all require either isolated dc power sources or a complicated voltage balancing circuit and control to support and maintain each voltage level [3].Three different major multilevel converter structures have been reported in this paper: cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped).Abundant modulation techniques have been developed.

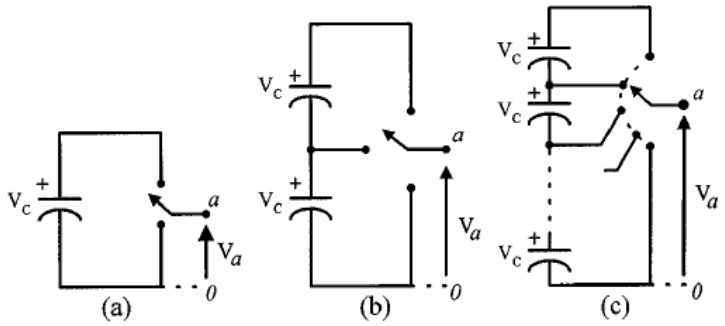

Fig 1: One Phase Leg Of An Inverter With (a) Two Levels (b) Three Levels (c) N Levels

Figure.1 shows a schematic diagram of one phase leg of inverters having various levels, for which the semiconductor act as an ideal switch for several positions.The two-level inverter provides an output voltage with two values (levels) with respect to the negative terminal of the capacitor [see Fig. 1(a)], while the three-level inverter generates three voltages, and so on. The most attractive features of multilevel inverters are as follows:

1. Generation of output voltages with extremely low distortion and lower $\frac{dv}{dt}$.
2. Drawing input current with very low distortion.
3. Generating smaller common-mode voltage, thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods,common mode voltages can be eliminated.
4. Operating with a lower switching frequency.

II. Topologies of Multi-Level Inverter

Diode-Clamped Inverter:

Operating Principle:

In Figure 2, 3-level and 5-level diode-clamped legs are shown; it is easy to extend the scheme to a generic n-level configuration. The DC bus voltage is split in sources are needed with respect to the standard 2-level inverter. The voltage between two switches is clamped through the diodes in the middle of the structure, called clamping diodes. Considering the 5-level diode-clamped leg, it is possible to note that the number of diodes required to clamp the voltage changes point by point. For instance D_1 is composed only by one diode; instead D_1' is the series of three diodes. This does not mean that the diode series connection is needed in the implementation, but it simply means that the reverse voltage drop born by D_1' is three times the backward voltage drop over D_1 . In the final implementation it is allowed to use either one diode with higher blocking capability or three diodes series connected. Anyway, to better understand how a diode-clamped works, it is preferred to use 26 series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor [4]. For a generic n-level diode-clamped the diode reverse voltage is given by (1.1):

$$V_r = \frac{E}{n-1} \qquad (1.1)$$

In 3-level diode-clamped it is V_r = E/2while in 5-level it is V_r = E/4. Furthermore, this voltage drop is also the reverse voltage each switch has to block. Now it is clear that increasing the levels means a reduction of the stress over the components, considering the same DC bus voltage. Unfortunately, higher is the number of levels higher is the number of components. Increasing of one level involve the use of one capacitor, two switches and a lot of diodes more. In fact the number of clamping diodes used in a diode-clamped is related to the number of level by the following expression:

$$N_{Diodes} = (n-1)(n-2) \qquad (1.2)$$

Focusing the attention to the 3-level leg, it is possible to find the relationship between the state of the switches and the output voltage V_{AO} . Before all consideration, a right switches configuration must avoid every kind of shortcut. So, it is simple to understand that all the switches cannot be be simultaneously turned on. There is also other dangerous configuration, but they can be avoided switching T_1 and T_1' in a complementary way. The same has to happen for T_2 and T_2'. Considering these conditions there are only four possible configurations a 3-level diode-clamped leg can assume and they are shown in Table 1 with the agreement to identify switches on-state with 1 and off state with 0. Not all the four configuration leads to a proper leg output voltage, because when T_1 in on and T_2 is off there is no defined path for the load current because whether T_2 or T_1' are not conducting, so the current flows throughout the free-willing diodes and the output voltage depends on it. As it is possible to see from Table 1, there are no intra-phase redundant states in 3-level diode-clamped [5].

Table1: 3-level diode-clamped leg relationships between configurations and output voltages

Switches state				
T_1	T_2	T_1'	T_2'	V_{AO}
1	1	0	0	E
0	1	1	0	$\frac{E}{2}$
0	0	1	1	0
1	0	0	1	Undefined

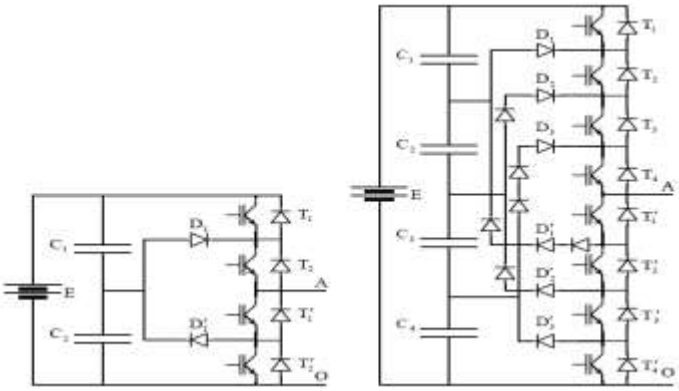

Fig 2: 3-level & 5- level diode-clamped legs.

Flying Capacitor:

Operating principle

In Figure 3, 3-level and 5-level flying-capacitor legs are shown and it can be seen a close similarity with diode-clamped topology. The extension to more than 5 levels is easy even for flying capacitor. As for the diodes in diode-clamped, the capacitors series are drown to highlight the voltage drop they have to tolerate. Indeed, the voltage over the capacitors nearer to the switches lowers than the voltage over the ones nearer to the source in steady-state. The voltage over each capacitor in Figure 3 is given by (1.3):

$$V_c = \frac{E}{n-1} \qquad (1.3)$$

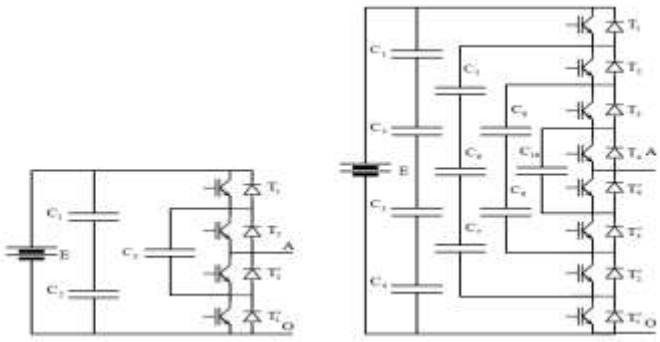

Fig 3: 3-level & 5-level flying capacitor leg.

Furthermore, these capacitors have the same function of the clamping diodes in diode-clamped converter: they keep constant the voltage drop between the busses to which they are connected. For this reason, they are called clamping capacitors. The voltage given by (1.3) is also the reverse voltage drop each switch must bear when all capacitors are fully charged as it can be seen applying Kirchhoff's voltage law to the circuit in Figure3. Like in every converter, some leg switches configurations are not allowed. For instance, considering the 3-level converter, T_2 and T_2' cannot be simultaneously closed because this means a shortcut of C_3. To avoid any problem coming from a possible shortcut of capacitors or sources, T_x and T_x' (where the subscript x substitutes the number of a generic switch) must to be in complementary state. In this way the possible configurations for n-level leg are:

$$N_{conf} = 2^{n-1} \qquad (1.4)$$

Obviously, flying-capacitor leg presents intra-phase redundancy because the number of allowed configurations is greater than the number of possible voltage output levels. In Table 2 the 3-level converter switching table is presented. For a 3-level flying-capacitor, there are 4 possible leg configurations and two of them give the same voltage level presenting intra-phase redundancy as expected. These two configurations have different effects on the capacitor C_3. Indeed, considering an outgoing output current, the configuration with T_1 turned off and T_2 turned on makes C_3 discharging because the capacitor has to feed the load .Whereas when T_1 is turned on and T_2 is turned off C_3 and the load are connected in series to the source and the current flowing into the capacitor charges it. A proper control can keep the capacitor balanced monitoring its space and choosing the right configuration each time the middle output is required [6].

Table2: 3-level flying capacitor leg relationships between configurations and output voltages

Switches state				
T_1	T_2	T_1'	T_2'	V_{AO}
1	1	0	0	E
1	0	0	1	$\frac{E}{2}$
0	1	1	0	$\frac{E}{2}$
0	0	1	1	0

Cascaded H-Bridge:

Operating principle

Figure 4 shows 3-level and 5-level cascaded H-bridge legs. As usual, the 3-level converter analysis is the simplest and let's understands the operating principle of the modules composing the leg of a generic n-level converter; these modules are often called cells. It is well known that H bridge converters can be modulated with 2-level or 3-level output. In this kind of multilevel converter, all the possible cell output levels are exploited. Some switches configurations are harmful for the converter and they must be avoided; for instance, the switches T_1 and T_1' are not allowed to be turned on at the same time because this situation causes a shortcut of the source. Table 3 shows the relationship between the allowed switches configurations and the output of a 3-level cascaded converter [7].

Table3: 3-level cascaded H-bridge leg relationships between configurations and output voltages

Switches state				
T_1	T_2	T_1'	T_2'	V_{AO}
1	0	0	1	E
1	1	0	0	0
0	0	1	1	0
0	1	1	0	-E

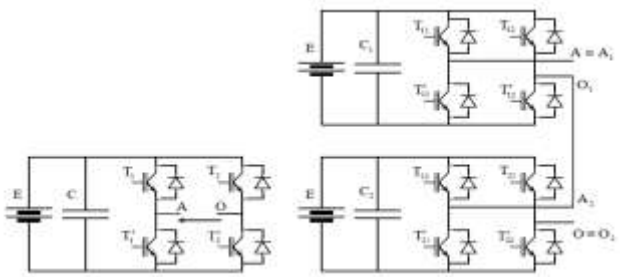

Fig 4: 3-level and 5-level cascaded H-bridge leg.

It can be seen that even cascaded converter presents an intra-phase redundancy because there are two different ways to obtain the level 0. Moreover, considering the same DC source voltage, the output level amplitude and the switches reverse voltage drop (given by (1.5)) are greater here than in the diode-clamped or flying-capacitor.

$$V_r = E \qquad (1.5)$$

In order to increase the number of levels more cells have to be cascaded. High and low couple of switches can be defined in the respect of voltage output direction. Considering Figure 4, the couple of switches composed by T_1 and T_1' are the high one, whereas T_2 and T_2' constitute the low couple. The high output of one cell is shortcut to the low output of another one to realize a cascade connection between two cells. . Each cell in the cascade adds 2 levels more to the output waveform [8].

III. Control Strategies

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage nearer to the sinusoidal wave. A large number of modulation techniques have been developed for harmonic reduction and minimization of switching loss. These modulation methods used in for multilevel inverters can be distinguinhed according to their switching frequency, as shown in Figure 5.

A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage. Another interesting alternative is SVC strategy, which has been used in three- level inverters. Fundamental switching frequency modulations produce switch commutations at output fundamental frequency and can be aimed to cancel some particular low frequency harmonic, SVC and SHE [9].

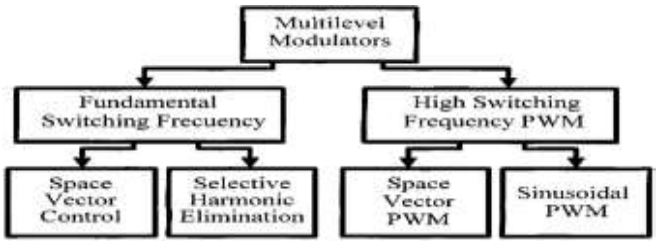

Fig 5: Classification tree for multilevel modulation

Multilevel Sinusoidl PWM

In SPWM we use several triangular carrier signals keeping only one modulating sinusoidal signals. If the level of inverter is m then (m-1) triangular carriers are needed .The frequency fc and peak to peak amplitude ac of all the carriers is same. The modulating signal is sinusoid of frequency fm and amplitude am. The carrier and the modulating signal are compared with each other in order to get on and off pulses. If the modulating signal is greater than triangular carrier, the switch is turned on otherwise it remains off.

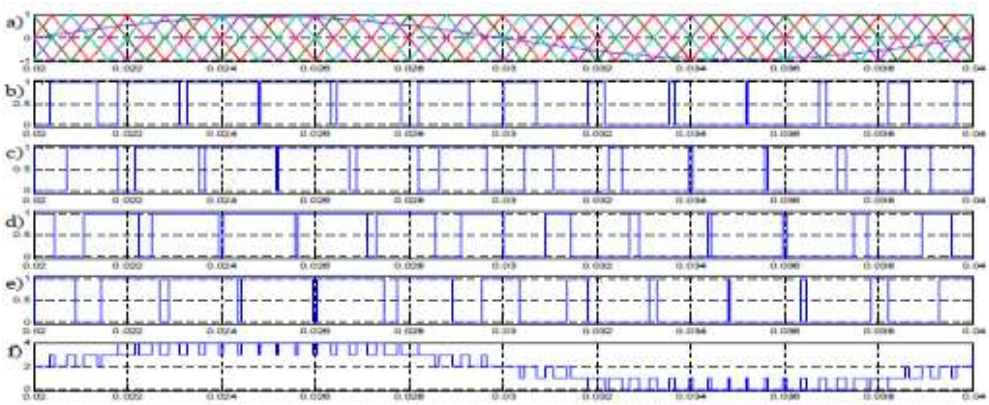

Fig 6 Various PWM Waveforms like Carriers and refrence; Comparison signals; Output waveform

Space Vector Modulation

In voltage space vector modulation we have to control the inverter output voltages in order that their Parks representation will be approximately equal to the reference voltage vector. If the level of the inverter is two then output of each phase will be either +Vdc/2 or – Vdc/2. SVM technique is easily applicable to all multilevel inverters. Figure.7 shows space vectors for the traditional two-, three-, and five-level inverters. The vectors are universal in nature and are applicable for all topologies. The adjacent three vectors can synthesize a desired voltage vector by computing the duty cycle (Tj, T_{j+1} and T_{j+2}) for each vector.

$$V^* = (TjVj + T_{j+1}V_{j+1} + T_{j+2}V_{j+2})/T$$

Space-vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). Due to these features it suitable for high-power and high-voltage applications.If the number of levels increases, redundant switching states and the complexity of selecting switching states also increases .Decomposition of the five level space-vector diagram into two three-level space-vector diagrams with a phase shift to minimize ripples and simplify control have been used by many authors [10].

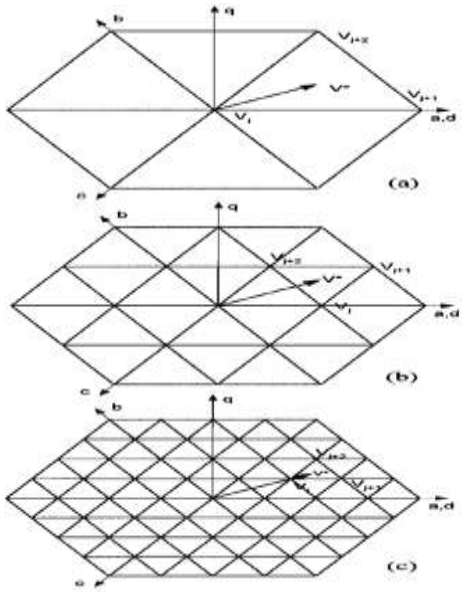

Fig 7: Space Vector Diagram (a) Two-level (b) Three-level (c) Five-level Inverter

Selective Harmonic Elimination-PWM

Selective Harmonic Elimination (SHE) is an off-line non carrier based PWM technique. In this scheme the basic square-wave output is "chopped" a number of times, which are obtained by proper off-line calculations. Figure.8 shows a generalized quarter-wave symmetric stepped voltage waveform synthesized by a (2m+1) -level inverter, where m is the number of switching angles. By applying Fourier series analysis, the amplitude of any odd n^{th} harmonic of the stepped waveform can be expressed as (4), whereas the amplitudes of all even harmonics are zero [11].

$$Hn = \frac{4}{n\pi}\sum_{k=1}^{m} vk \cos(nak) \qquad (1.6)$$

where V_k is the K^{th} level of dc voltage, n is an odd harmonic order, m represents the number of switching angles, and a represents the switching angle. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to m-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. To keep the number of eliminated harmonics at a constant level, all switching angles must be less than $\frac{\pi}{2}$.

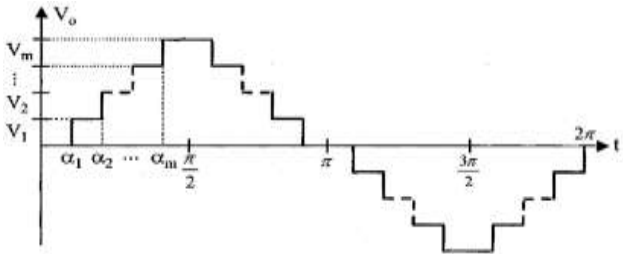

Fig 8: Generalized Stepped Voltage Waveform

However, if the switching angles do not satisfy the condition, this scheme no longer exists. As a result, this modulation strategy basically provides a narrow range of modulation index, which is its main disadvantage [12].

Space Vector Control

A conceptually different control method for multilevel inverters, based on the space-vector theory, has been introduced. This control strategy, called SVC, works with low switching frequencies and does not generate the mean value of the desired load voltage in every switching interval, as is the principle of SVM.

Figure.9 shows the 311 different space vectors generated by an 11-level inverter. The reference load voltage vector V_{ref} is also included in this figure. The main idea in SVC is to deliver to the load a voltage vector that minimizes the space error or distance to the reference vector V_{ref}. The high density of vectors produced by the 11-level inverter (see Fig.9) will generate only small errors in relation to the reference vector; it is, therefore, unnecessary to use a more complex modulation scheme involving the three vectors adjacent to the reference [13].

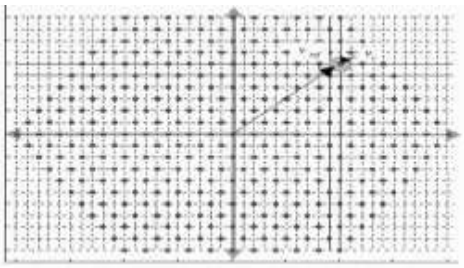

Fig 9: Load Voltage Space Vectors Generated By An 11- Level Inverter

The shaded hexagon of Figure.9 shows the boundary of highest proximity, which means that when the reference voltage V_{ref} is located in this area, vector V_c must be selected, because it has the greatest proximity to the reference.Figure.10 (a) presents the voltage generated by one cell in an eleven-level multi cell inverter with five cells per phase and an output frequency of 50 Hz. The load voltage of the inverter for the same frequency and modulation index 0.99 is shown in Figure.10 (b).

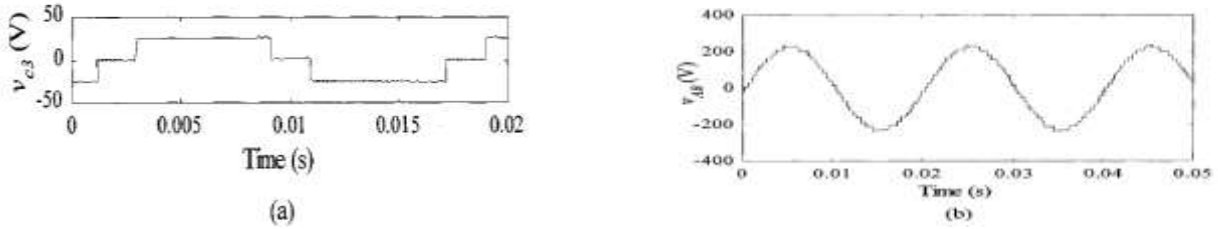

Fig 10: Voltages generated by an 11- level inverter with SVC (a) One Cell Voltage (b) Resulting Load Voltage

VII Literature Review

Yuan Xiaoming (2000), reported that the conventional diode clamping inverter suffers from such problems as dc link unbalance, indirect clamping of the inner devices, turn-on snubbing of the inner dc rails as well as series association of the clamping diodes etc. It is due largely to these problems that the application of the conventional diode clamping inverter in practice has been deterred, in spite of being discussed in the academia. A new diode clamping inverter, which works without the series association of the clamping diodes was discussed in this paper. An auxiliary resistive clamping network solving the indirect clamping problem of the inner devices was also discussed for both the new and conventional diode clamping inverter. The existing multilevel inverters such as diode-clamped and capacitor-clamped multilevel inverters can be derived from the generalized inverter topology. Moreover, the generalized multilevel inverter topology provides a true multilevel structure that can balance each dc voltage level automatically without any assistance from other circuits, thus, providing a complete and true multilevel topology that embraces the existing multilevel inverters. From this generalized multilevel inverter topology, several new multilevel inverter structures can be derived**.** This generalized multilevel converter topology has a niche for implementing magnetic less, compact, high-efficiency, zero-EMI, and low-cost power conversion [14].

Seo Jae Hyeong et. al., (2001)," reports a simplified space –vector pulse width modulation (SVPWM) method for three level inverter. This method was based on the simplification of the space vector diagram of a three level inverter into that of a two level inverter. In the field of high power, high performance applications, the three level inverter proved to be the most promising alternative [16]. THE SVPWM method has the following features:

1. The switching sequence is determined without a look up table, so the memory of the controller can be saved.
2. The dwelling times of voltage vectors are calculated at the same manner as two level SVPWM. Thus the method reduces the execution of the three level SVPWM.
3. It is easy to implement the neutral-point potential control algorithm.

Marabeas Pantelis, et. al., performed a comparison between existing multilevel inverter topologies. The topologies examined were the Neutral Point ClampMultilevel inverter (NPCMLI) or Diode-Clamped Multilevel Inverter (DCMLI), the Flying Capacitor Multilevel Inverter(FCMLI) and the Cascaded Cell Multilevel Inverter (CCMLI). The comparison of these inverters was based on the criteria of output voltage quality (Peak value of the fundamental and dominant harmonic components andTHD), power circuitry complexity, and implementation cost [17].

Zhang Yongchang et. al., (2011) reports a hybrid PWM , combining the merits of both space vector PWM (SVPWM) and selective harmonic elimination (SHE) PWM. SHEPWM was made actually for three-level neutral point-clamped (NPC) inverter-fed high power adjustable speed drives, which has used asynchronous SVPWM at low frequency and SHEPWM at high frequency. A general formula used in obtaining the initial switching angles for three –level inverter was illustrated in this paper. The characteristics of the multiple solutions in three level SHEPWM ,in terms of their harmonic performances and pulse widths were comparatively investigated and then applied in the design of a high–power industrial drive [18].

Najafi Ehsan et.al., (2012), proposed that multilevel inverters have been widely accepted for high-power, high-voltage applications. Their performance was highly superior to that of conventional two-level inverters due to reduced harmonic distortion, lower electromagnetic interference and higher dc link voltages. In this paper, a new topology with a reversingvoltage component was used. This topology has used fewer components compared to existing inverters (particularly in higher levels) and fewer carrier signals and gate drives. Therefore, the overall cost and complexity were greatly reduced particularly for higher output voltage levels. This topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS etc. Here, the switching operation was separated into high and low frequency parts which will add up to the efficiency of the converter as well as reducing the size and cost [19].

Zhiguo Pan, et al., presented a new voltage balancing control for the diode-clamped multilevel rectifier/inverter system. A complete analysis of the voltage balance theory for a five-level back to- back system is given.The proposed control strategy regulates the dc bus voltage, balances the capacitors, and decreases the harmonic components of the voltage and current. Grain P. Adam, et al., introduced a new operational mode for diode-clamped multilevel inverters termed quasi two-level operation. Such operation aims to avoid the imbalance problem of the dc-link capacitors for multilevel inverters with more than three levels and reduces the dc-link capacitance without introducing any significant voltage ripple at the dc-link nodes. Z. Oudjebour, et al., used the stabilization of the input DC voltages of five-level flying capacitors (FLFC) voltage source inverters (VSI) . A feedback control algorithm of the rectifier is proposed. N. A. Azli, et al., addressed Implementation of a regular sampled PWM technique based on a single carrier multilevel modulation strategy on a multilevel inverter using a digital signal processor (DSP). José Rodríguez, et al., addressed a switching strategy for multilevel cascade inverters, based on the space-vector theory. The proposed switching strategy generates a voltage vector with very low harmonic distortion and reduced switching frequency [14-19] .

Conclusion

This paper has been addressed a survey of several technical literature concerned with Multilevel Inverter Topologies and their Modulation Techniques. It also concludes that by applying control strategies on MLI the harmonics can be reduced to a greater extent. This paper does not contain all the research, references or the related work but it can introduce the researchers with the fundamental principle of the MLI. Authors strongly believe that this survey article will be very much useful to the researchers for finding out the previous work done in the field of MLI topologies and their modulation techniques.

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