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Single Phase Neutral Point Diode Clamped Active Rectifier - A Literature Review

Naveesh Kant Sharma[1], Susheva Sharma[2], Vikrant Sharma[3], Ashish Sharma[4]
[1,2,3]M. Tech Scholar, Electrical Engineering, Lovely Professional University, Punjab, India
[4]Asst. Prof. & COD, Electrical Engineering, Lovely Professional University, Punjab, India
[1]sharma.naveesh68@gmail.com, [2]sushevasharma@gmail.com

Abstract: The ac-dc conversion is used increasingly in a wide diversity of applications: power supplies for microelectronics, household electric appliances, electronic ballasts, battery charging, dc motor drives, power conversion, etc. As shown in figure below ac- dc converters can be classified to different topologies working with low switching frequency (line commutated) and other topologies which operate with high switching frequency. The simplest line-commutated converters use diode to transform the electrical energy from ac to dc. In this paper the analysis of single-phase neutral point active rectifier is proposed to reduce harmonics from the supply and also to achieve unity power factor. Here different PWM techniques are used and the line current command is derived from a Dc link voltage regulator and an output power estimator. The hysteresis current controller is used to track the line current command. To balance the neutral point voltage, a capacitor voltage compensator is employed.

Keywords: Neutral Point Diode Clamped Rectifier, PWM, Harmonics.

I. Introduction

The main goal of electric utility is to deliver sinusoidal voltage at fairly constant magnitude throughout the system the loads connected to the system complicate these objectives by producing harmonic currents. These harmonic currents lead to distorted voltages and currents that have an adverse impact on the power system performance. Therefore while making any additions or changes to an installation two concepts should be taken into considerations:

1. Nature of harmonic-current producing loads (Non Linear Loads).
2. The way in which harmonic currents flow and hoe the resulting harmonic voltages develop.

II. Effect of harmonics

1. Losses and overheating in transformers shunt capacitors, power cables. AC machines and switchgear, leading to premature aging and failure.
2. Excessive current in the neutral conductor of three-phase four-wire systems, caused by odd triplet current harmonics (triplet: 3^{rd}, 9^{th}, 15^{th} etc). This leads to overheating of the neutral conductor and tripping of the protective relay.
3. Fuses and circuit breakers: harmonics can cause false or spurious operations and trips, damaging or blowing components for no reason.
4. Reduced power factor, hence less active power available from a wall outlet having a certain apparent power rating.
5. Electrical resonances in the power system, leading to excessive peak voltages and RMS currents and causing premature aging and failure of capacitors and insulation.
6. Premature failure of SMPS and uninterruptible power supplies (UPSs).failure of sophisticated electronics equipments like computers, remote monitoring systems, air conditioning systems etc.

III. Need for Active Rectifiers

The optimal ac/dc converter would be one in which output is a pure dc voltage (or current) and the input would draw a pure sinusoidal current at unity power factor from the ac lines. Traditionally, the converters were designed to meet the needs of dc side and trhe little attention was paid to the input power factor of the converter. The problems created by the current harmonics inti the ac lines and operating the converter at low power factor well known. Many techniques hve been propsed which can be classified as follows:

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1) Passive input filter techniques
2) Active filter techniques
3) New circuits and control techniques(Active Rectifiers)

The first two methods concern the suppression of the undesired effects of a standard bridge converter, while the last techniques reflects an intent to minimize the harmonics created by the converter and operate it at power factor. In this paper diffent control strategies have been discussed for single phase neutral point diode clamped active rectifier to reduce the harmonics and improve the power factor.

IV. Classification Of Converters System

Classification is based on the converter used as shown in Fig1 . these are broadly classified into two types, namely, unidirectional and bidirectional converters:

Unidirectional converters are realized using a diode bridge in conjunction with other power electronic converters, namely, step-down chopper. Step-up chopper, Step-up/down chopper, isolated, forward, flyback, push pull, half bridge, bridge, SEPIC, Cuk, Zeta, etc., and multilevel convertors. Bidirectional ac-dc convertors consists of basic convertors normally used in invertors such as push-pull, half bridge, voltage- source invertors, current- source invertors employing MOSFETs for low-power , IGBTs for medium-power, and GTOs for high-power convertors. These ac-dc convertors are extensively employed for adjustable –speed drives used to drive active loads such as a hoist, a crane, traction, etc., line interactive UPS, and BEES. Four-quadrant ac-dc convertors are normally implanted using matrix convertors.

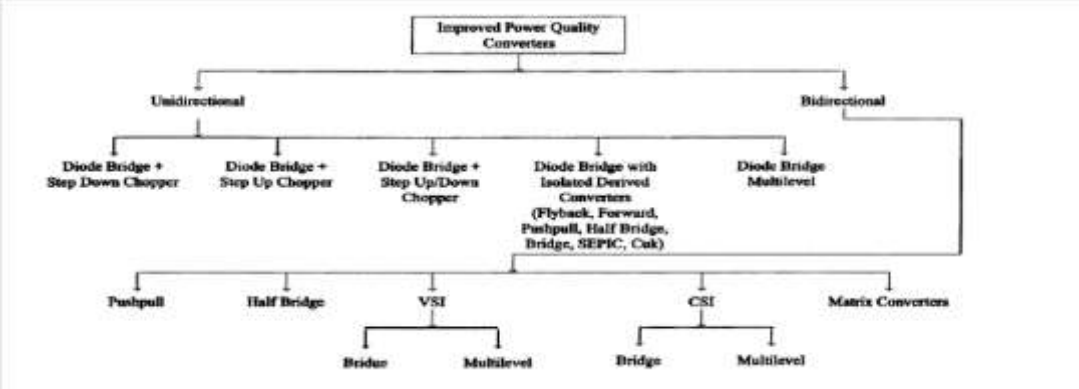

Fig 1: Classification of Converters

Multilevel convertors have the advantages of low stresses on the device, low losses and thus high efficiency and are suitable for high-power applications. It has a stepped voltage wave form instead of PWM and has reduced high-frequency currents. The switching frequency of high power semiconductors switches is usually limited by maximum power loss. According to the voltage level of the power semiconductor, there are two-level and multilevel pulse-width modulation (PWM) schemes the two-level and three-level PWM pattern. The voltage stress of power switches can be reduced significantly if the voltage levels are increasing, but the circuit complexity, voltage balance problem and control and control scheme become more difficult.

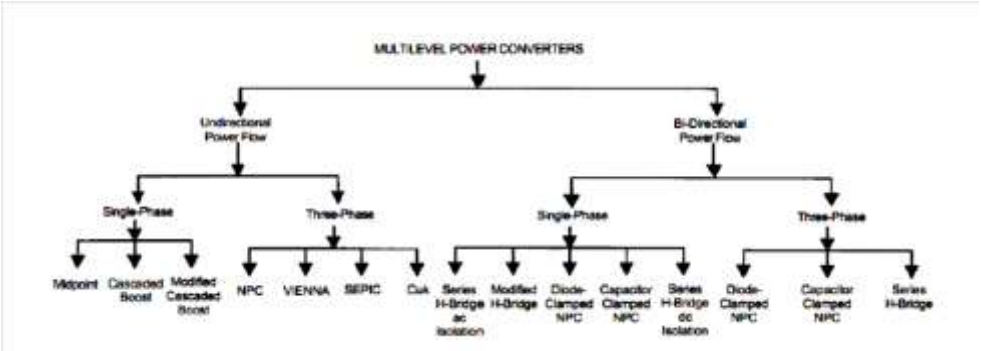

Fig 2: Classification of Multilevel Power Converters

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V. Single Phase Neutral Point Diode Clamped Active

Fig 2 shows the proposed neutral-point diode-clamped rectifier to draw a sinusoidal line current with low harmonic content and high power factor. the circuit configuration consists of one boost inductor L, two DC-bus capacitors C1 and C2, two power diodes D3 and D4, two neutral-point clamped diodes D1 and D2, four power switches T1-T4 with anti parallel diodes. The voltage stress of the power switches equals half of the DC-bus voltage. A hysteresis current controller is used in the inner control loop to track the line current command. To achieve a DC-link voltage, a proportional-integral voltage controller is employed in the outer control loop to generate line current command and balance the active power between the mains and the DC load. A capacitor voltage compensator is adopted to perform neutral point voltage compensation. By appropriate control 5 different voltage levels v_{dc} ,v_{dc} /2 ,0, -$v_{dc,}$ -v_{dc} /2 are generated on the AC side of the adopted converter. Based on the proposed control aalgorithm, the power factor of the system will be improved.

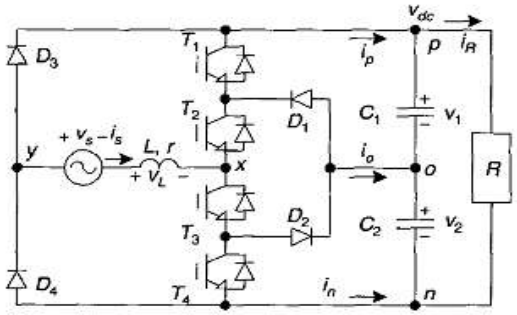

Fig.2 Circuit configuration of neutral-point diode-clamped rectifier

a) PRINCIPLE OF OPERATION

There are six operational modes in the proposed rectifier based on the line current and switching states of power switches as shown in Table. For positive line current, modes 1,2 and 3 are employed in the proposed control algorithm to generate rectifier terminal voltage vxy=vdc vdc/2 and 0 respectively (assuming v1= v2= vdc/2) Modes 4, 5 and 6 are adopted to achieve vxy=0, - vdc/2 and -vdc respectively ,in the negative line current. The following analysis of the modes of operation assumes that the power switches are ideal, the supply voltage is constant value during one switching period, and that v1= v2= vdc/2

Mode 1: Fig.3 shows the equivalent circuit of first operational mode. In this mode no power switch is turned on and positive line current charges both capacitor voltage v1 and v2 to achieve voltage vxy=vdc . The line current is decreasing in this mode because vs< vdc. The DC side currents are $i_p = i_s$, $i_0 = 0$, $i_n = i_s$.

Mode 2: The equivalent circuit is shown in Fig.3 Power switch T3 and diodes D2 and D4 are turned on to obtain voltage vxy= vdc/2 voltage. The positive line current charges capacitor C2. The Dc load current also discharges capacitor C1 and C2. The boost inductor voltage equals vs -vdc/2. The DC side currents are $i_p = 0$, $i_0 = i_s$, $i_n = i_s$.

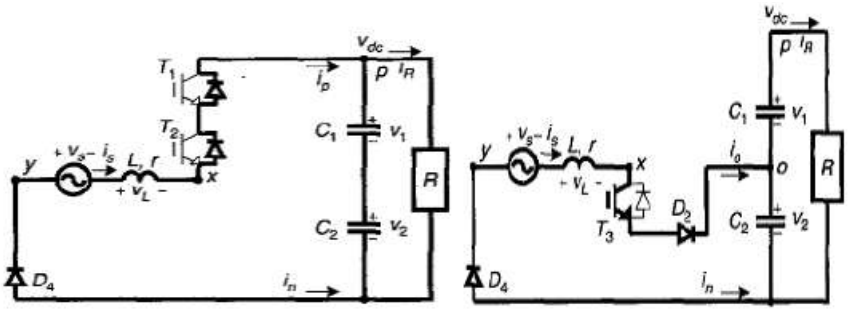

Fig.3 Operation in a) mode - 1 & b) mode - 2

Mode 3: The equivalent circuit of operation mode 3 is given in Fig.4 Power switches T3 and T4 and diode D4 are turned on to achieve voltage v_{xy} = 0. The line current is linearly increasing because $v_L = v_s > 0$. In this mode, two capacitors voltages are decreased to supply the DC load.

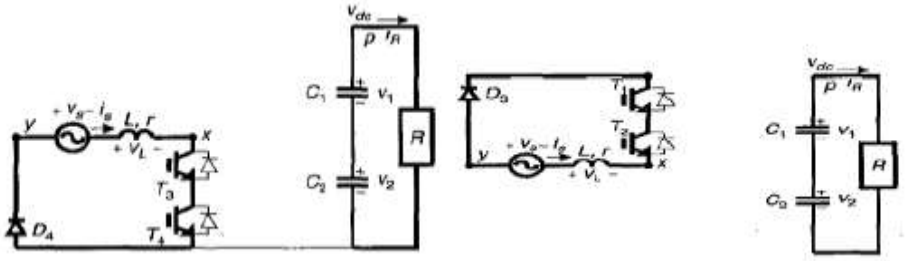

Fig.4 Operation in a) mode-3 & b) mode-4

Mode 4: The line voltage is short-circuited through the boost inductor in mode-4 as shown in Fig.4 power switches T1 and T2 and diode D3 are turned on to obtain voltage v_{xy}= 0. the inductor current is linearly decreasing because $v_L = v_s$ <0, The Dc load current discharges capacitors C1 and C2. The dc side currents are $i_p=i_o=i_n=0$

Mode 5: The equivalent circuit of mode 5 is shown in Fig5. Power switch T2, and diodes D1 and D3 are turned on to obtain voltage $v_{xy}= -v_{dc}/2$. The negative line current charges capacitor C1. The boost inductor voltage equals. Capacitors C1 and C2 are also discharged by the DC load. The DC side curren $i_p=i_s,i_o=i_s,i_n=0$

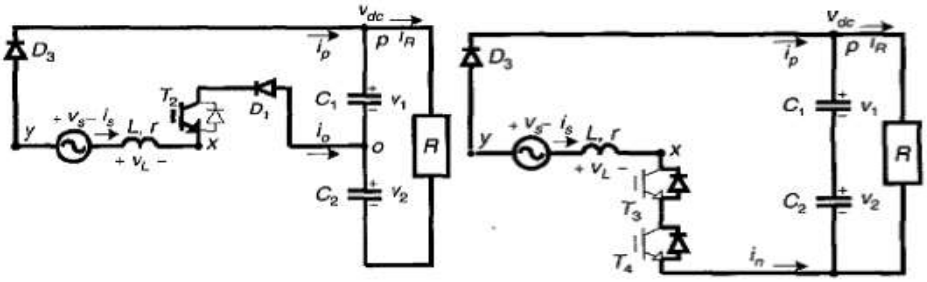

Fig.5 Operation in a) mode-5 & b) mode-6

Mode 6: Fig.5 shows the equivalent circuit of operation mode 6. In this mode all power switches are turned off and negative line current charges both DC-bus capacitors to achieve voltage $v_{xy}= -v_{dc}$. The line current is increasing in this mode because $v_s + v_{dc} > 0$. The DC- side currents are $i_p= -i_s$, $i_0= 0, i_n= i_s$

According to this analysis of the six operational modes, the DC-side current ip, does not equal zero in modes 1,5 and 6. The neutral-point current io is not equal to zero in modes 2 and 5. The DC-side current in is not equal to zero in modes 1, 2 and 6. These DC-side currents can be expressed as a function of switching states and the direction of line current.

$$i_p = T_1' T_2' T_3' T_4' \frac{1+\text{sgn}i_s}{2} i_s - T_1' T_3' T_4' \frac{1-\text{sgn}i_s}{2} i_s \quad (1)$$

$$i_o = T_1' T_2' T_3 T_4' \frac{1+\text{sgn}i_s}{2} i_s + T_1' T_2 T_3' T_4' \frac{1-\text{sgn}i_s}{2} i_s \quad (2)$$

$$i_n = -T_1' T_2' T_4' \frac{1+\text{sgn}i_s}{2} i_s + T_1' T_2' T_3' T_4' \frac{1-\text{sgn}i_s}{2} i_s \quad (3)$$

Where sgn i_s = 1(or -1) if i_s >0 (or i_s<0). The Ac-side voltage of the proposed rectifier vxy can be expressed by the Dc-bus voltage, line current and switching states of power switches.

$$v_{xo} = (T_1' T_2' T_3' T_4' v_1 + T_1' T_2' T_3' T_4' v_2) \frac{1+\text{sgn}i_s}{2} + (T_1 T_2 T_3' T_4' v_1 + T_2 T_3' T_4' v_2) \frac{1-\text{sgn}i_s}{2} \quad (4)$$

$$v_{yo} = (v_1 + v_2) \frac{1-\text{sgn}i_s}{2} \quad (5)$$

$$v_{xy} = (T_1' T_2' T_3' T_4' v_1 + T_1' T_2' T_3' T_4' v_2) \frac{1+\text{sgn}i_s}{2} + [(T_1 T_2 T_3' T_4' - 1) v_1 + (T_2 T_3' T_4' - 1) v_2] \frac{1-\text{sgn}i_s}{2} \quad (6)$$

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According to the switching states of the power switches, five voltage levels v_{dc} ,v2,0 are generated on the voltage v_{xy} . To obtain a balanced neutral-point voltage, capacitor voltages v1 and v2 are controlled to be equal.

VI. CONTROL STRATEGIES

TWO-LEVEL PWM CONTROL STRATEGY

Based on the proposed control scheme, the proposed rectifier is controlled to draw a sinusoidal line current with almost unity power factor. For two-level unipolar PWM modulation, the switching waveforms of the proposed rectifier are shown in Fig 6 . The rectifier terminal voltage v_{xy} equals v_{dc} (mode 1), 0, (mode 6). In two-level unipolar PWM, the power circuit of the rectifier can be expressed as a second-order system and given as

$$v_s = ri_s + L\frac{di_s}{dt} + uv_{dc} \qquad (7)$$

$$ui_s = 0.5C\frac{dv_{dc}}{dt} + i_R \quad (C_1 = C_2 = C) \qquad (8)$$

Where u = 1,0 or -1. In the positive mains voltage, modes 1 and 3 are used to control line current and to generate voltage v_{xy} = 0,respectively. Modes 4 and 6 are adopted in the negative mains voltage to achieve AC-side voltage v_{xy} =0 and – v_{dc} respectively. A phase – locked loop circuit and a voltage controller are used to generate the line current command. A hysteresis current comparator is employed to control the line current command in phase with the mains voltage. Based on the line current error and the sign of the mains current, the corresponding switching functions of the power switches are expressed as:

$$T_1 = T_2 = [1 - \text{hys}\Delta i_s]\frac{1 - \text{sgn}i_s}{2} \qquad (9)$$

$$T_3 = T_4 = \text{hys}\Delta i_s\frac{1 + \text{sgn}i_s}{2} \qquad (10)$$

The corresponding waveforms and control strategy are

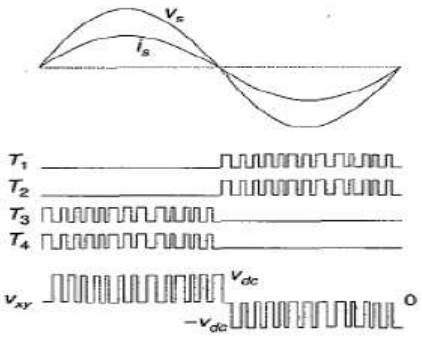

Fig 6. Switching-signals and ac side voltages of two-level PWM Rectifier

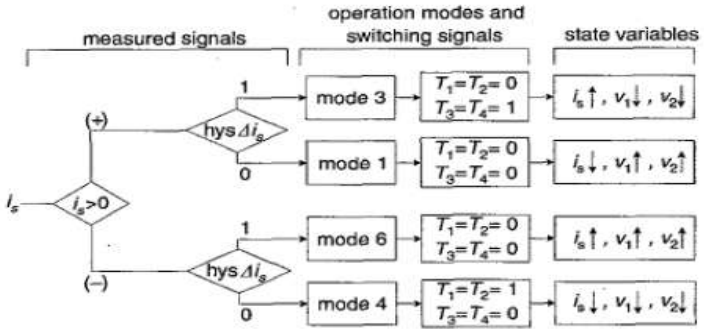

Fig 7. Control strategy (two-level PWM)

The control block of the unipolar PWM of the proposed rectifier is shown in Fig 8

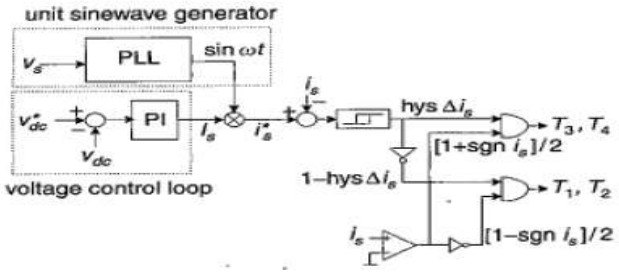

Fig 8. Control block diagram (two level PWM)

Three-Level PWM Control Strategy

For three-level PWM modulation, a neutral- point voltage $v_{dc}/2$ is generated to achieve a three-level voltage pattern on the rectifier ac-terminal voltage. The more voltage levels generated on the Ac side of the rectifier, the less voltage harmonics are produced by the rectifier. The features of three-level PWm modulation of the proposed rectifier are drawing ca clean sinusoidal line current with unity power factor, maintaining constant Dc-link voltage, and keeping a balanced neutral-point voltage. To generate a three-level voltage waveform on the AC side of the rectifier, two operation regions of the mains voltage during one cycle of the input line frequency are defined and shown in Fig 9. in the first region,the line voltage is greater than $– v_{dc}/2$ and less than $v_{dc}/2$. Voltage levels 0 and $v_{dc}/2(-v_{dc}/2)$ are generated on the voltage v_{xy} in the positive (or negative) mains voltage to control the line current. In the second region, the absolute value of the mains voltage is less than the DC-bus voltage but greater than half the DC-link voltage $v_{dc}/2$. Voltage levels v_{dc} and $v_{dc}/2$ (- v_{dc} and-$v_{dc}/2$) are generated in the positive (or negative) half-cycle of the line voltage to track the line current. These operation regions and the corresponding PWM voltage waveforms are shown in FIG.9 In the positive half-cycle of the mains voltage, power switches T1 and T2 are turned off. Power device T3 or T4 is turned on or off to generate voltage $v_{xy} = v_{dc}/2$ or 0 respectively. Modes 2 and 3 can be employed to generate these two voltage levels. No power switch is turned on to achieve voltage $v_{xy} = v_{dc}$ in the positive line current. The voltage levels v_{dc}(mode1), $v_{dc}/2$(mode 2) and 0(mode 3) are generated on the voltage v_{xy} in the positive mains voltage because line current is controlled to have zero phase shift. The line current is controlled to increase (or decrease) in mode 3(mode 2) if mains voltage is less than neutral-point voltage $v_{dc}/2$ i.e in region 1. Mode 1 or mode 2 is used to decrease or increase the mains current in the condition of $v_{dc}<v_s<-v_{dc}$(region 2)

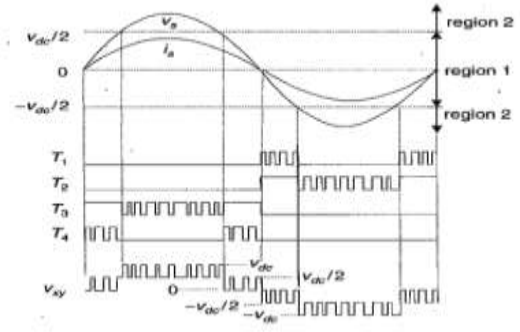

Fig 9. Switching signals and Ac-side voltage of three-level PWM Rectifier

Based on this above analysis, the line current is controllable in the positive mains voltage by using modes 1,2 and 3. For the negative mains voltage ,power switches T3 and T4 are turned off. Modes 4 and 5 as shown above are employed to obatain voltage $v_{xy} = 0$ and $– v_{dc}/2$ in the first region. In mode 4 the line current is decreasing because boost inductor voltage v_L is equal to the mains voltage v_s. The line current is increasing in mode 5 because $v_L = v_s$ +vdc/2 >0. In the second region, modes 5 and 6 are adopted to achieve voltage levels $–v_{dc}/2$ and $–v_{dc}$ on the rectifier AC terminal voltage. The line current is controlled to increase or decrease by using mode 6 or mode 5. Three voltage levels 0(mode 4),-$v_{dc}/2$(mode 5)and $–v_{dc}$(mode 6) are generated in the negative half-cycle of the mains voltage. Based on this the rectifier analysis, the inductor current variation, DC-link voltage and rectified supply voltage are given , the proper operational mode can be chosen to control the inductor current. Fig4.9 gives the control strategy of the proposed rectifier to perform three-level PWM. First the sign of the main current is detected. Modes 1, 2 and 3 are used in the positive line current and modes 4,5 and 6 are adopted in the negative mains current. To properly control the line current a region detection of the mains voltage is performed to select the appropriate mode.

$$T_1 = [1 - \text{hys}\Delta i_s][1 - \text{comp}(|v_s| - v_{dc}/2)]\frac{1 - \text{sgn}i_s}{2} \quad (12)$$

$$T_2 = [1 - \text{comp}(|v_s| - v_{dc}/2)]\frac{1 - \text{sgn}i_s}{2} + [1 - \text{hys}\Delta i_s] \cdot \frac{1 - \text{sgn}i_s}{2} \quad (13)$$

$$T_3 = [1 - \text{comp}(|v_s| - v_{dc}/2)]\frac{1 + \text{sgn}i_s}{2} + \text{hys}\Delta i_s \cdot \frac{1 + \text{sgn}i_s}{2} \quad (14)$$

$$T_4 = \text{hys}\Delta i_s \cdot [1 - \text{comp}(|v_s| - v_{dc}/2)]\frac{1 + \text{sgn}i_s}{2} \quad (15)$$

where

$$\text{comp}(x) = \begin{cases} 1, & \text{if } x \geq 0 \\ 0, & \text{if } x < 0 \end{cases} \quad (16)$$

In region 1, operation modes 2 and 3(or modes 4 and 5) are used in the positive (or negative) cycle of the mains voltage. In region 2, modes 1 and 2 (or modes 5 and 6) are employed in the positive (or negative) mains voltage. A hysteresis current comapartor is used to track the line current command. Based on the control strategy of three-level PWm shown in Fig 10. the switching functions of power switches are expressed as shown:

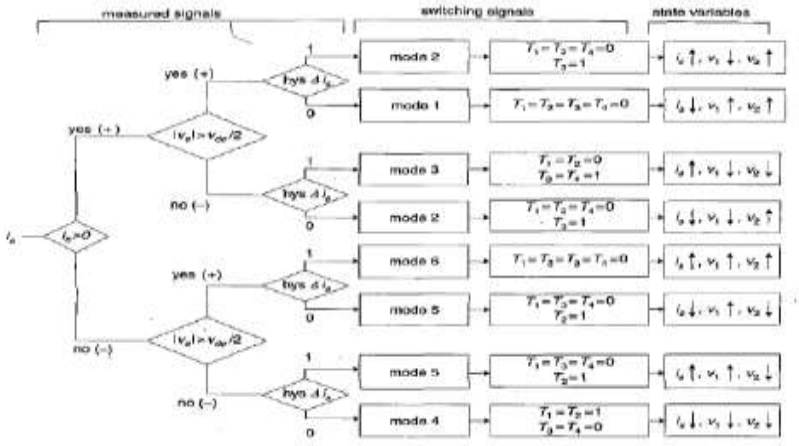

Fig10. Control strategy (three-level PWM)

Fig 11 shows the control block diagram of the proposed rectifier for three-level PWM. A proportional-integral voltage controller is employed in the outer loop control to maintain the constant DC-link voltage for balancing the real power between the mains and the DC load. Once the main voltage or DC load has changed , the real power between the load and the mains is not sustained. The real main power is changed by adjusting the line current command to compensate the rea power charged or discharged by the DC capacitor and to match the real power variation of the load. The linear current command is derived from the output of the voltage controller and the phase-locked loop circuit. The phase-locked loop circuit generates a unit sinusoidal wave in phase with the mains voltage. To balance the neutral-point voltage, the voltage variation between the two capacitors is added to the line current command. The sensed line current is compared with the line current command i_s*. an inner current loop control based on a hysteresis current comparator is used to track line current command. According to the measured line current error and the detected mains voltage, the corresponding switching signals of the power switches based on equations are generated to obtain three- level voltage pattern on the AC side of rectifier. If the power switches in the proposed rectifier are ideal the voltage stress of each power switches equals half the DC-bus voltage

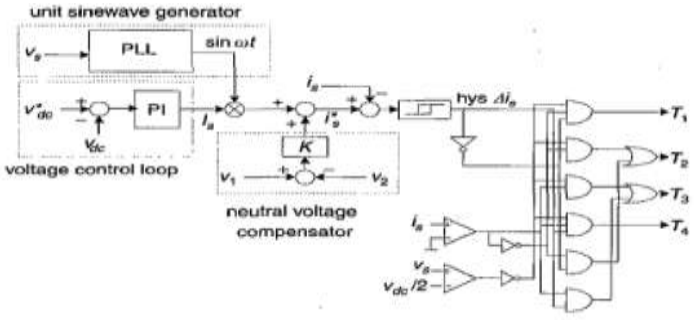

Fig.11. Control block diagram (three-level PWM)

The control scheme of single-phase neutral point diode clamped rectifier is to achieve a unity input power factor. Proportional-integral(PI) voltage controller, neutral point voltage compensator and a hysteresis current comparator are employed to perform dc-link voltage regulation, neutral point voltage balance and line current tracking respectively.

VII. LITERATURE REVIEW

Kinck Eugenio Werne et.al. (1991), "A high frequency AC/DC converter with unity power factor and minimum harmonic distortion". In this paper a new force commutated AC/DC converter and control strategy was proposed that was able to draw nearly sinusoidal currents at unity poer factor from three-phase power lines. Here the poor factor was controlled by adjusting the relative position of the fundamental component of an optimized PWM typed voltage with respect to the supply voltage. Current harmonic distortion is minimized by the use of optimized firing angles for the converter at a frequency where GTO's can be used. Thus, the converter has the ability to operate at unity poor factor with low current distortion which is ideal for the power supply system. Chen Der-Jan et.al.,(2001), "High power factor single phase neutral point diode clamped rectifier". In this paper a controlled algorithm for single phase neutral point diode clamped was proposed to achieve unity power factor, low harmonic distortion, balanced neutral point voltage and constant dc bus voltage. Four power switches were used in the proposed rectifier to generate two-level unipolar PWM or three-level PWM wave form on the rectifier terminal voltage. The main advantages of the adopted rectifier were generating high voltage pattern using the low voltage stress devices and reducing the harmonic contents. Lin Bor-Ren et.al.,(2002), "Single-phase Neutral point diode clamped rectifier with high input power factor". In this paper a new controlled scheme for single-phase neutral point diode clamped rectifier was proposed to achieve a unity power factor and low harmonic distortion. Four power switches were used in the proposed rectifier to generate two-level unipolar PWM or three-level PWM wave form on the rectifier terminal voltage. The hysteresis current controller was used to track the line current command and a capacitor voltage compensator was employed to balance the neutral point voltage. Thus, improving the power factor and reducing the harmonic contents. Lin Bor-Ren et.al.,(2002), "Half bridge neutral point diode clamped rectifier for power factor correction". In this paper a high power factor rectifier based on neutral point clamped scheme was proposed to achieve unity input power factor and balanced neutral point voltage. The hysteresis current control scheme (carrier less PWM scheme) was employed to draw a clean sinusoidal line current, high input power factor, regulated dc link voltage and balanced voltage capacitor. By using this scheme the voltage stress of power devices on the proposed rectifier was reduced with that of the conventional half bridge and full bridge PWM rectifiers. The voltage harmonics generated by proposed rectifier were less than that of the half bridge rectifiers. Marchesoni Mario et.al.,(2005), "A new control strategy for neutral point clamped active rectifier". In this paper a new control strategy was developed for interfacing a neutral-point clamped active rectifier with the mains. In this a method based on the modulation of the input current amplitudes was proposed to compensate the dc- link capacitors voltages fluctuations. When a real neutral point clamped converter is developed, the neutral point voltage exhibits an unstable behaviour that must be avoided in all operating conditions, here the dc link capacitor voltage fluctuations in a neutral point clamped active rectifier is compensated which permits achieving a correct capacitor voltage sharing also in no-load condition when conventional method fail.

Conclusion

The various aspects harmonics and poor power factor are discussed in this paper.Authors strongly believe that this survey will be very much useful to the researchers for finding out the previous work done in the field of rectifiers.This paper will be helpful for the researchers for studying the various aspects of Single phase neutral point diode clamped active rectifier.

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