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Comparison and analysis of sequential circuits using different logic styles

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Abstract: In digital VLSI, power dissipation has become a prime constraint. Many design architecture and techniques have been developed to reduce power dissipation. In this paper implementation of sequential circuits such as D flip flop, PIPO shift register and RAM in Gate diffusion input (GDI) technique and its comparison with other logic styles is presented. This technique allows reduced power consumption and delay while maintaining low complexity of logic design. The design is simulated using Mentor Graphics Design Architect.

Keywords: VLSI; CMOS; Pass Transistor Logic (PTL); Gate Diffusion Input (GDI); Parellel In Parellel Out (PIPO); RAM.

I. INTRODUCTION

Technology scaling has become a primary driver of the electronics industry and has provided a path towards both denser and faster integration. With continuous aggressive technology scaling it is difficult to sustain supply and threshold voltage scaling to provide the required performance increase, limited energy consumption, control power dissipation and maintain reliability. So in order to reduce power consumption different design techniques have been developed [1].

One form of logic that is popular in low-power digital circuits is pass transistor logic. Advantages of PTL include high speed, lower power dissipation and lower interconnection effects. Certain drawbacks of PTL are overcome by GDI technique. This allows implementation of a wide range of complex logic functions using only two transistors. It is also suitable for design of fast, low power circuits, reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving power characteristics.

In this paper, analysis and comparison of D Flip flops, PIPO shift registers and RAM using different design techniques are performed and simulated in Mentor Graphics Design tool. Different design style includes CMOS logic, double pass transistor logic (DPL), and transmission gate (TG) and Gate diffusion input logic.

Section II presents comparison of different logic styles. In section III brief introduction of GDI cell is discussed. Section IV shows the discussion of sequential circuits such as D flip flop, shift register and memory. Section V presents results and discussions. Conclusion is discussed in section VI.

II. COMPARISON OF DIFFERENT LOGIC STYLES

The comparison were carried out for CMOS,double pass transistor, transmission gate and gate diffusion input(GDI) logic styles. Complementary CMOS logic style-Conventional or complementary CMOS are built from an nmos pull down or a dual pmos pull up logic network.Any logic functions can be realized by nmos pull down and pull up network connected between the gate output and power line. Advantages of CMOS style are its robustness and transistor sizing and thus reliable operating at low speed. In spite of these advantages there are certain drawbacks such as slowest speed and high power consumption [2].

Pass transistor logic style-One form of logic design that is popular is pass transistor logic. The basic difference between pass transistor logic and CMOS logic style is that the source side of the logic transistor network is connected to some input signal instead of power lines. Advantages of PTL include high speed, lower power consumption and lower interconnect effect. In spite of these advantages there are certain drawbacks such as slower operation and reduced voltage swing [2]. Different types of pass transistor logic styles are there which include complementary pass transistor logic, double pass transistor logic, single rail pass transistor logic etc.

Double pass transistor logic (DPL) uses complementary transistors to keep full swing operation and reduce the dc power consumption. One disadvantages of DPL is the large area used due to the presence of pmos transistor.

Transmission gate (TG) logic-The most widely used solution to deal with the voltage drop by pass transistors is the use of transmission gates. It uses transmission gate logic to realize complex function using less number of transistors.

Gate diffusion input (GDI)-It is new low power design techniques that solves the problem of CMOS and pass transistor logic. This technique allows reduced transistor count, power consumption, delay and area when compared with other logic styles.

III. GDI CELL

A new low power design technique namely gate diffusion input technique allows implementation of a wide range of combinatorial synchronous function using only two transistors. This method is found to be suitable for design of fast, low power circuits using only two transistors (as compared to CMOS and existing PTL techniques), while simultaneously improving logic level swing and static power characteristics and allows simple top down design methodology [3]. The GDI method is based on the use of simple cell as shown in Fig 1.At first glance the basic cell resembles the standard CMOS inverter, but there are important differences: GDI cell contain three inputs. G (the common gate input of the nMOS and pMOS transistors), P (input to the outer diffusion node of the pMOS transistor) and N (input to the outer diffusion node of the nMOS transistor). The out node (the common diffusion of both transistors)may be used as input or output port depending on circuit structure.

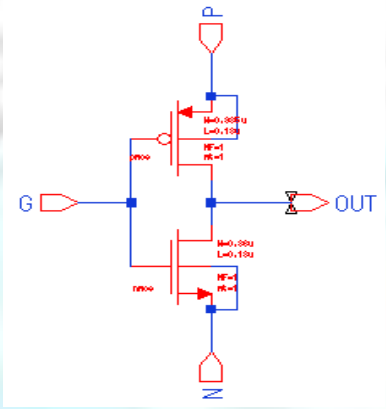

Fig 1: GDI cell

The various functions that can be implemented with basic GDI cell are as shown in Table I.

TABLE I: FUNCTIONS THAT CAN BE IMPLEMENTED USING BASIC GDI CELL

N	P	G	OUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	FUNCTION 1
B	1	A	A’+B	FUNCTION 2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+AC	MUX
B’	B	A	A’B+B’A	XOR
B	B’	A	AB+A’B’	XNOR

IV. SEQUENTIAL CIRCUITS

In digital circuit theory, sequential logic is a logic circuit whose output nit only depends not only on the present value of its input signals but on the past history of the inputs. This is in contrast with the combinational circuits, in which whose output depends only on the present input. That is, sequential circuit has memory while combinational circuit does not .Or, in other words sequential circuit is combinational logic with memory. Sequential logic is used to construct finite state machine a basic building block in all digital circuitry as well as memory circuits and other devices. Virtually all circuits in practical digital devices are a mixture of combinational and sequential circuits. Examples of sequential digital circuits are flip flops, shift registers, counters etc.

A. D FLIP FLOP

Flip flop and latches are used as data storage element. Such data storage can be used for storage of states; such storage is described as sequential logic. When used in finite state machine, the output and next state depends not only on its current input, but depends on its current state. Flip flops can be either simple or clocked; the simple ones are commonly called latch. The word latch is commonly used for storage elements, while clocked devices are described as flip flops.

D flip flop is widely used, it is also known as data or delay flip flop. The D flip flop captures the value of the D input at a definite portion of the clock cycle. The captured values become the Q output. At other times the output Q does not change. The D flip flop can be viewed as a memory cell. In this paper flip flop is compared with other logic styles with respect to no: of devices, power dissipation and delay [4]. Fig 2, 3, 4 and 5 shows D flip flop using different logic styles.

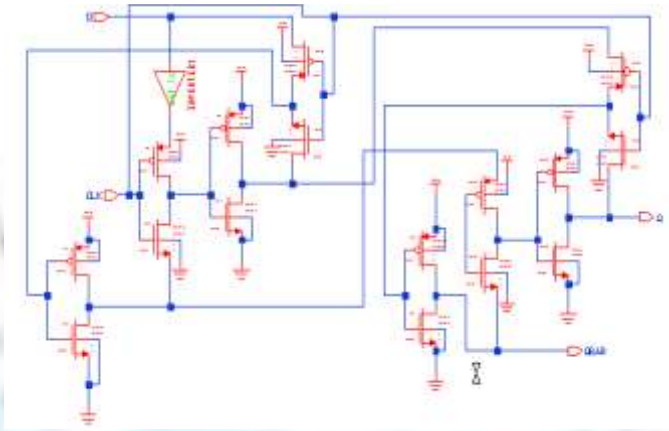

Fig 2: D Flip flop using GDI

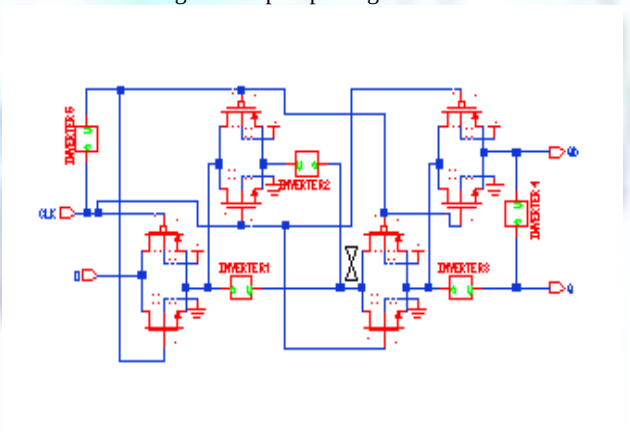

Fig 3: D Flip flop using Transmission gate

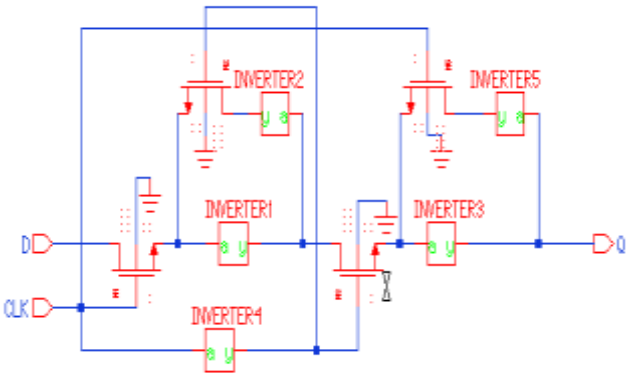

Fig 4: D Flip flop using pass transistor

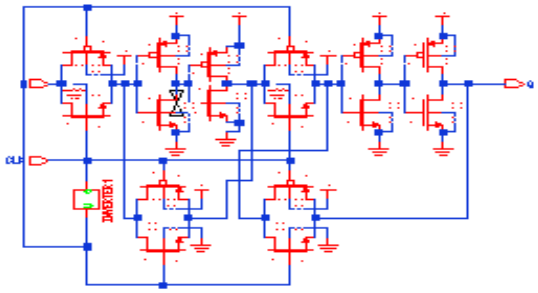

Fig 5: D Flip flop using CMOS

B. SHIFT REGISTERS

In digital circuits, shift registers is a group of flip flops used to shift or transfer data from one flip flop to other flip flop. It's a group of D flip flops connected in a chain and a clock of flip flop is connected in a synchronous manner. Basic functions of shift register include data storage and data movement. Different types of shift registers are there namely: Serial in Serial out (SISO), Serial in Parallel out (SIPO), Parallel in Serial out (PISO) and Parallel in Parallel out (PIPO).

For Parellel in Parellel Out shift registers all date bits appear in parallel outputs immediately following the entry of the data bits. The D's are the parallel inputs and Q's are the parallel outputs. Once the register is clocked all the data at the input appears at the output simultaneously. Fig 6 shows schematic of GDI shift register using D flips flop. If we replace the D flip flop using other logic style, then shift register using different logic styles can be obtained.

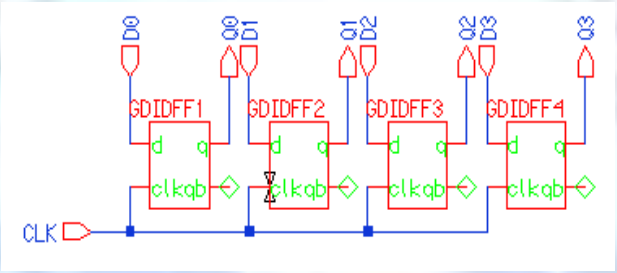

Fig 6: Schematic of PIPO shift register using GDI

C. RANDOM ACCESS MEMORY (RAM)

A memory unit is a collection of storage cell together with associated circuits needed to transfer data in and out of the device. The internal construction of random access memory of m words with n bits per word consists of mxn binary storage cells and the associated logic for selecting individual words [5].The binary storage cell is the basic building block of the memory cell. Binary cell which is capable of storing one bit of information is shown in fig 7.SR latch is used to model the storage part of the cell. One bit of information is stored in its internal latch. Reading and writing operation is enabled by the select input, the read and write input determines the operation by forming path from latch to the output terminal. A 0 in the read or write input provides the write operation by forming a path from input to latch.

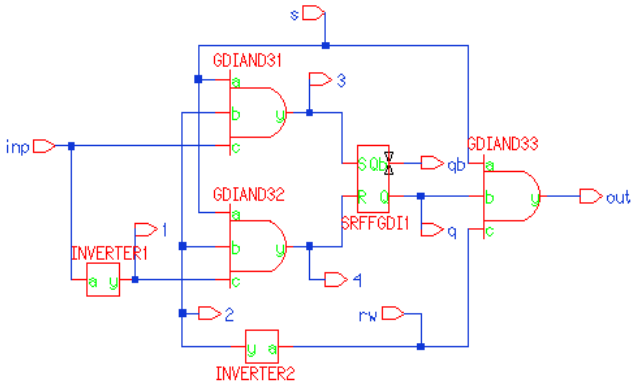

Fig 7: Schematic of binary storage cell

The schematic of 4x4 RAM is shown in the fig 8.This RAM consists of four words of four bits each and has a total of 16 binary cells. The binary cell has three inputs and one output. The memory with four words needs two address lines. The two address line goes through 2x4 decoder to select one of the four words. The decoder is enabled with the memory enable input. When the memory enable is 0, output of the decoder is 0 and none of the memory word is selected. With memory select 1, one of the four words is selected according to the value of address lines. Once a word is selected, the read/write determines the operation.

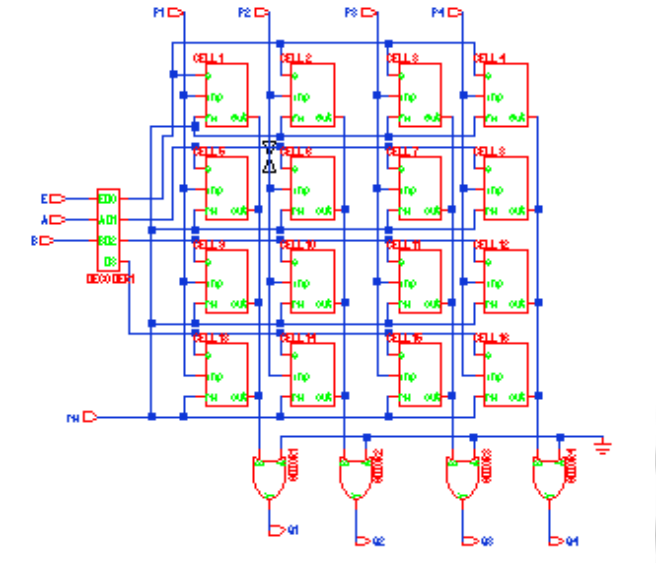

Fig 8: Schematic of 4x4 RAM using GDI

During the read operation, the four bits of the selected word go through OR gates to the output terminal [6]. During the write operation, the data available in the input lines are transferred to the binary cells of the selected word. The binary cells that are not selected are disabled and their previous binary values are unchanged. When the memory select input goes into the decoder is equal to 0, none of the words are selected and the contents of the cell remain unchanged regardless of the read/write input.

V. RESULTS AND DISCUSSIONS

D Flip flops, PIPO shift registers and RAM memory are implemented using four different logic styles such as CMOS; double pass transistor, transmission gate and gate diffusion input. Comparisons are based on the performance parameter such as number of transistors and power consumption. Simulations were carried out using Mentor Graphics Design Architect in 130nm technology. To achieve low power and high performance these circuits were tested at 0.8V to 1.8V.

The comparative results for D flip flop for different logic design styles are given in Table III. From the table we can see that GDI technique is having reduced delay and power consumption. Shift registers are formed by cascading the D flip flop. Table IV shows comparative results of PIPO shift register using different design styles. As in the case of D flip flop shift register using GDI is having reduced power consumption when compared with other design styles. Finally the comparative result of RAM using GDI and CMOS is shown in Table V. A bar graph is plotted for power dissipation of flip flops and shift registers for the logic in Fig 9 and Fig 10 respectively.

TABLE III: Comparative analysis of D flip flop using different logic styles

	Logic Style	Power(nW)	Delay(pS)	No:of transistors
D flip flop	GDI	3.9979	160.66	18
	CMOS	5.8171	229.84	18
	PTL	5.8251	188.01	14
	TG	5.8131	194.59	18

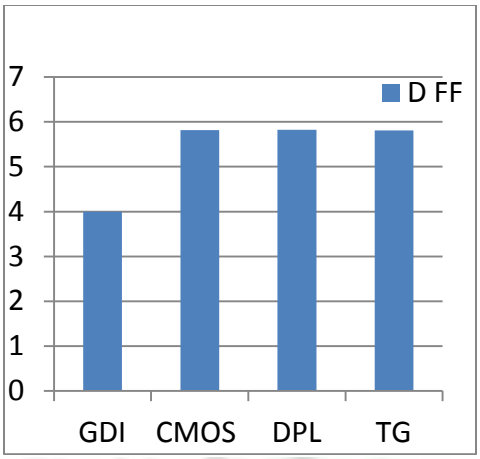

Fig 9: Power comparisons of D flip flop

TABLE IV: Comparative analysis of 4 bit PIPO shift registers using different logic styles

	Logic style	Power(nW)	Delay(pS)	No: of Transistors
Shift register	GDI	17.8148	501.43	72
	CMOS	29.1357	499.11	72
	PTL	30.2875	501.10	56
	TG	29.1355	499.06	72

TABLE V: Comparative analysis of transistor count of RAM using GDI and CMOS design styles

	Logic styles	No: of transistors
RAM	GDI	412
	CMOS	636

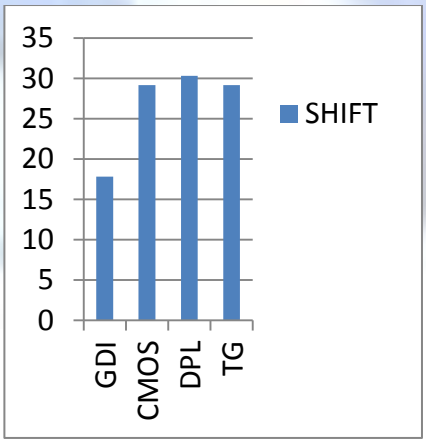

Fig 10: Power comparison of PIPO shift register

VI. CONCLUSION

In this paper, D flip flops, shift registers and memory based on four different logics were designed and the results were compared. The four different logic styles are Gate diffusion input, CMOS, Double pass transistor and transmission gate. It has been observed that Gate diffusion input (GDI) design style exhibit better characteristics as compared to other design style. Gate diffusion input design style can be considered to be the best logic design style with respect to parameters such as power, and delay. So, Gate diffusion input design style can be used in low power and high performance applications.

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