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A review on microprocessor with multi-core

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ABSTRACT: As we know that Microprocessors is a device which can perform the operation in microseconds. Each generation of processors grows a small type, but faster dissipated more heat and more consumed the power. A number of techniques such as data levels of parallelism, instruction levels of parallelism, thread level parallelism and simultaneous multi threading (SMT) already exists which make the big improvement in the performance of microprocessor cores. This paper present evolution of different types of microprocessor and multi-core processor followed by introducing the technologies and its advantages in modern world and also explain the currently challenges faced by multi-core processors and microprocessors.

KEYWORDS: Microprocessor, Core Processors, multi threading technologies, software challenges hardware parallelism, and High performance computing (HPC), SMT.

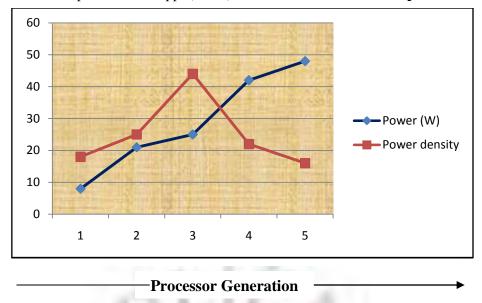
1. INTRODUCTION

The Industry of microprocessor continues to have great valuable in the course of technological advancements since their existence in 1970s [1]. The improving market and the demand for faster performance drove the industry to manufacture faster and smarter chips. One of the most classical and given techniques to improve performance is to clock the chip at higher frequency which enables the processor to execute the programs in a much quicker time [2, 3] and the industry has been following this trend from 1983-2002 [4]. Additional techniques have also been devised to improve performance including parallel processing, data level parallelism and instruction level parallelism which have all proven to be very effective [5]. One such technique which improves significant performance boost is multi-core processors. Multi-core processors have been in existence since the past decade. Around 1945, mathematician John von Neumann with John Mauchly creating of an Electronic Discrete Variable Automatic Computer, more famously known as the EDVAC. The Von Neumann suggested the stored-program model of computing. In the architecture of von Neumann, the sequence of instructions is known as program which is stored sequentially in the memory of computer. The program's instructions are executed one after the other in a linear format; single-threaded manner [7]. At present Von Neumann architectures are widely used class of architectures because of their relative simplicity and effectiveness for general computation tasks like in architecture family of IBM series [6]. As time went on, advancements in mainframe technology expanded upon the ideas presented by von Neumann. In the 1960s saw the advent of timesharing operating systems. Run on large mainframe computers, these operating systems first introduced the of concurrent execution of program. Many numbers of users could access simultaneously a single mainframe computer and submit jobs for processing. The operating system handled the details of allocating Central Processing Units (CPU) time for each individual program. At this time, concurrency existed at the processing level, and this type of job of task switching was left to the systems making programmer [1].

2. EVOLUTION OF MULTI-CORE PROCESSOR

The microprocessors have always been designed for their performance and cost keeping in mind. Gordon Moore who was the founder of Intel Corporation predicted that the number of transistors on a chip will almost be double once in every two year to meet this ever growing demand which is popularly known as Moore's Law in the semiconductor industry [3, 9, 10]. In present days the integrated circuit processing technology increasing integration density which has made it possible to integrate one billion transistors on a single chip for the improved performance [8,11]. However, the performance increase by micro-architecture governed by Pollack's rule is roughly proportional to square root of increase in complexity [12]. This would mean that doubling the logic on a processor core would only improve the performance by 42%. In advanced fabrication chip techniques there is big problem of bottleneck, power dissipation issues. From studied on it we can say that the transistor leakage current increases as the chip size reduced further and it will increases the static power dissipation to large values as shown in figure1 below [12, 13]. There is one change means to improve the performance and is to increase the frequency of operation which makes it fast execution of programs [3, 10]. As we increases the frequency beyond this limit it will increases power dissipation again [1].

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Figures1: Power density rising [16]

As we know that in single core contained in a single core CPU there is register files attached with ALU (arithmetic logic unit) both connected to bus interface. In case of multi-core CPU (central processing unit) there are many cores are contained in CPU with bus interface device, known as multi-core architectures. In the multi-core CPU chip all the cores fit on single processor socket which known as chip multi processor (CMP). One is dual core processor architecture is known as advanced micro devices (AMD) released on 22 April, 2005 and dual core processor athelon which is known as athelon 64 x2 family released on 31 May, 2005 in the term of architecture. [20]

3. THE MULTICORE PROCESSORS

General trend in computer architecture shifts towards more parallelism. Instruction level parallelism which is at the machine-instruction level, the processor can reorder, pipeline instruction, split them into microinstruction. ILP enabled rapid increases in processor speeds over the last 16 years. Thread level parallelism (TLP) is a parallelism on coarser scale. Using TLP a computer game can do graphics, algorithm and physics in three separate threads. Next step is multi core architecture explicitly exploiting TLP [27]. The most recent advances in microprocessor design for desktop computers involve putting multiple processors on a single computer's chip. These types of multicore designs are completely replacing the ordinary type single core designs that have been the foundation of desktop computers. Multicore processor is the most recent evolution in computing technology [28]. A multi-core processor is composed of two or more independent cores. It can be defined as an integrated circuit which has two or more individual processors called cores. Designer typically integrates the cores into a single integrated circuit die known as a Chip Multiprocessors (CMPs) [26]. A dual- core processor contains two cores are Intel Pentium Dual-Core and 4(quad) core processor contains four cores which is also known as Intel Core Duo, like Intel 2010 core line, which also includes 3 levels of 4(quad) core processors, and a 6(hexa) core processor contained six cores is Intel Core i7 Extreme Edition 980X which is high performance general purpose processor in all respects and this processor dissipate maximum (140W) power [16]. A multi-core processor implement multiprocessing in a single physical package. Designer can be couple cores in a multi-core device together loosely or tightly [26]. In example, we can say that cores may be or may not be share caches, and they may be implement messages passing or memory shared by them inter-core communication methods. The Core Duo multicore processor was introduced in 2006 and offered for multiple cores with lower power consumption. Intel's Core 2 Duo is one of Intel series of multicore processors. Multicore processors are enhanced with hyper threading, giving each core two logical processors. The first of Intel's multicore processors was Intel Pentium processor Extreme Edition, in April of 2005. It had dual cores and supported hyper threading, giving the system eight logical cores and it has no hyper threading but supports 64 bit architecture [26]. In the present digital world, the requirements for complex 3-Dimensional simulations, brooking media files, added levels of safety, more interacted user interfaces, big databases, and more on-line users are beginning to extended single-core processor capabilities. Multi-core processors enable true multitasking. On single-core systems, multitasking can be maximize the CPU utilization, consequential that decreased performance as operations have

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to wait to be processed. In multi-core systems, each core has its own cache; the operating system has sufficient property to handle most compute exhaustive tasks in parallel [30]. However, In the case of multi-core processors if you have multitasks that can be run in parallel at the same time, each of them will be executed by a separate core in parallel thus improving the performance as shown in figure 2 [17].

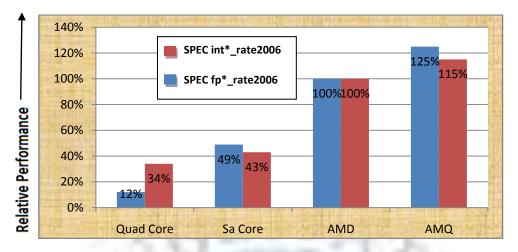


Figure 2: Multi-core chips performance [17]

The multi-cores inside the chip are not clocked at a higher frequency, but it replaced their capacity to execute programs in parallel is what at first contributes to the overall performance making them more energy efficient and low power cores as shown in the figure below [5]. Multi-core processors are generally designed in separation so that the cores which are unused can be powered down or powered up as and when needed by the application contributing to overall savings of power dissipation.

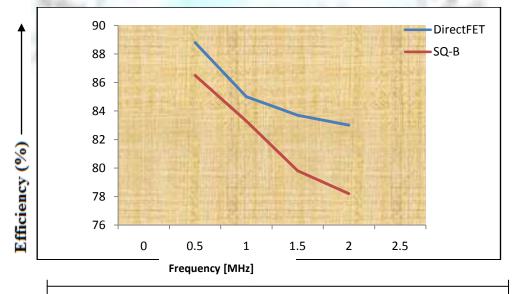


Figure 3: Dual core at 20% reduced clock frequency with a single-core at maximum frequency [5]

Multi-core processors could be implemented in many ways based on the application requirement. It could be implemented either as a group of heterogeneous cores or as a group of homogeneous cores or a combination of both [25]. In homogeneous core architecture, all the cores in the CPU are identical [18] and they apply divide and different approach to improve the overall processing to break up a high computationally intensive application into less computationally intensive applications and execute them in parallel [6]. Other major benefits of using a homogeneous multi-core processor are reduced design complexity, reusability, reduced verification effort and hence easier to meet time to market criteria [19]. On the other hand heterogeneous cores consist of dedicated application specific processor cores that would target the issue of running variety of applications to be executed on a computer [6]. As an example could be a DSP core addressing multimedia applications that require typical mathematical calculations, a

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complex core addressing computationally intensive application and a remedial core which addresses less computationally intensive applications [7]. However it was observed that there is no any type of improvement while executing sequential programs on multi-core chips due to under use of cores. Compilers are being developed which parallelize applications automatically so that multiple independent tasks can run simultaneously on different cores. [11]

MEMORY SYSTEM

If we design a uniprocessor, the memory system consists of one or more caches to feed into the single processor with data and instructions. Different cores have different levels of cashes shown in the figure4 below. With multi-cores, the caches are just having one part of the system of memory; the other components include the, cache coherence support, and the intrachip interconnection. These determine how cores can communicate impacting ability of programming, parallel of application performance, and the number of cores that the system can adequately support. Each core uses the memory as monolithic array which is shared by all the cores as shown below [27]. SMT is a technique complementary to multi-core; it can have one large and superscalar core and great performance on single thread as compared to the multi-core which is great with the TLP. In the memory hierarchy SMT shared all caches [27].

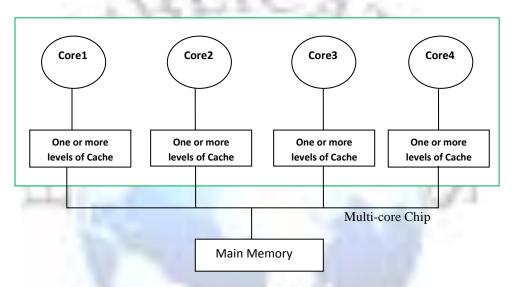


Figure 4: Different cores with their level of cache with main memory

4. APPLICATIONS

The benefit from multi core is data servers, web servers or in other words we can say that these are used in web commerce. The multi-cores are also used in scientific techniques like CAD/CAM. These are used in multimedia techniques. For example in photo editor when we record a Television show through a digital video recorder and in case of downloading software while running an anti-virus program. All others many more things which we are can be threaded in present days and we can map them efficiently with the help of multi cores [27].

5. CHALLENGES FACED BY MULTI-CORE PROCESSORS

In case of microprocessor the processing is in normal condition and the CPU can perform operation easily. In case of many advantages of multi-core processors, there are a few major challenges are facing with the technology. A major issue is seen with regard to software programs execute slower on multi-core processors as compared to single core processors. It can be correctly pointed out that "As cores are increased, then the applications on multi-core systems don't get faster automatically" [11]. Programmers can be write applications that make use of the increasing number of processors in case of a multi-core environment without stretch the time needed to software developing [15]. Many of applications used now a day were written to execute on a single processor only, which is fail to use the capability of multi-core processors [21]. But the software companies can develop software programs capable to utilize the multi-core processor to the fullest, the critical challenges the industry faces is how to port birthright software programs

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developed to multi-core aware software program [21]. Re-designed programs although possible, in today's environment it is really not a technological decision. It's more of a commercial decision when the companies have to decide whether to go re-designing the software programs keeping the key parameters such as customer satisfaction, time to market, and cost reduction [21].

The industry is present this problem by designing the compilers which can port the birth light single core software programs to 'multi-core' programs which will be capable of using the power of multi-core processors. The compilers could be perform "reordering code", where the compilers will generate, reordering code instructions such that instructions that can be run in parallel are close to each other [13]. This would able us to instructions are execute in parallel improving performance. Also compilers are developed to generate parallel threading or processing automatically for application which are given so that these processing can be executed in parallel [13]. Intel released major updates for "C++" tools which seemed at program makers exploiting parallelism in multi-core processors. Also alongside Open Multiprocessing, an application programming interface which supports multiprocessing programming in "C" and "C++" provides directives for much type of threaded codes [22]. It has been pointed that "when application code is multi-core ready then the energy efficiency and multitasking performance of multi-core processors will all be fully realized."

The second, on-chip interconnections are becoming a crucial bottle-neck in meeting performance of multi-core chips [23]. The processor's performance truly depends on how fast a CPU can sense the data rather than how fast it can operate on it to avoid data hunger scenario [26]. With increase the number of cores comes along the high interconnect delays when data is to be moved across the multi-core chip from memories in particulars [24]. Smarter integration and Buffering of memory and processors are a few classic techniques which have attempted to present this issue [25]. Another important feature which impacts multi-core performance is the interaction between cores, memory controller's viz. on chip components and cache and memories viz. shared components [11] where bus latency and contention are the key area of concern. Mesh techniques or Special crossbars have been implemented on hardware to present this issue [11].

Another major's challenge is use of simultaneous multi threading (SMT) which can permits independent threads to execute simultaneously on the same core. For example if one thread is waiting for floating point operation to complete it then another thread can use the integer units. But without SMT only a single thread can run at any given time. SMT not a true parallel processor because it can only enable better threading up to 31% if we compare it with multi core each core has its own copy of resources. In case of multi core threads can run on separate cores. When we want to programming for multi core it must be use threads or processes, we divide the workload across multiple cores and then write the parallel algorithm [27].

6. CONCLUSION

In this paper after deep study of microprocessor with multi cores the author concluded that the performance improvement to be gained from using some faster mode of execution. Multi-core chip is an important new trend in computer architecture. Several new multi-core chips in design phases. Parallel programming techniques likely to gain importance. It appears that the evolution of these multi-core architectures will finally force a radical change in how applications are programmed. Specifically, developers must be considering how to direct the collaboration of many concurrent threads of execution to solve a single problem. Power and frequency limitations observed on single core implementations. However the complete performance can be realized only when the challenges multi-core processors facing today are fully addressed. A lot of technological trends are expected in this area of technology including a new multi-core programming language. There is considerable amount of research going on, in the field of multi-core processors more efficiently.

REFERENCES

- [1]. Aspray, W. 1997, "The Intel 4004 microprocessor: what constituted invention?", Annals of the History of Computing, IEEE, vol. 19, no. 3, pp. 4-15.
- [2]. Sodan, A., Machina, J., Deshmeh, A., Macnaughton, K. & Esbaugh, B. 2010, "Parallelism via Multithreaded and Multicore CPUs", Computer, vol. PP, no. 99, pp. 1-1.
- [3]. Parkhurst, J., Darringer, J. & Grundmann, B. 2006, "From Single Core to Multi-Core: Preparing for a new

- Vol. 2 Issue 8, Sept.-Oct., 2013, pp: (17-23), Available online at: **www.erpublications.com** exponential", Computer-Aided Design, 2006. ICCAD '06. IEEE/ACM International Conference on, pp. 67
- [4]. Goodacre, J. & Sloss, A.N. 2005, "Parallelism and the ARM instruction set architecture", Computer, vol. 38, no. 7, pp. 42-50.
- [5]. R. Ramanathan. Intel multi-core processors: Making the move to quad-core and beyond. Technology@Intel Magazine, Dec 2006.
- [6]. Dezso. Sima. Terence Fountain. Peter Karsuk: Advanced Computer Architectures-A Design Space Approach.
- [7]. S. Akhter, and J. Roberts, (2006); "Multi-Core Programming (Increasing Performance through Software Multi-threading)" Published by Richard Bowles, Library of Congress Cataloging in Publication Data, Printed in the United States of America.
- [8]. Lizhe Wang, Jie Tao, Gregor von Laszewski, Holger Marten. 2010, "Multicores in Cloud Computing: Research Challenges for Applications", Journal of Computers, Vol 5, No 6 (2010)
- [9]. Schaller, R.R. 1997, "Moore's law: past, present and future", Spectrum, IEEE, vol. 34, no. 6, pp. 52-59.
- [10]. Cass, S. (2010). Multicore Processors Create Software Headaches. Technology Review, 113(3), 74-75.
- [11]. Lance Hammond, Basem A. Nayfeh, Kunle Olukotun, "A Single-Chip Multiprocessor," Computer, vol. 30, no. 9, pp. 79-85, Sept. 1997
- [12]. S. Borkar. "Thousand core chips A technology perspective".DAC'07: Proc. of the 44th annual Conf. on Design Automation, pages 746–749, 2007
- [13]. Roy, A., Jingye Xu & Chowdhury, M.H. 2008, "Multi-core processors: A new way forward and challenges", Microelectronics, 2008. ICM 2008. International Conference on, pp. 454.
- [14]. Brooks, D.M., Bose, P., Schuster, S.E., Jacobson, H., Kudva, P.N., Buyuktosunoglu, A., Wellman, J., Zyuban, V., Gupta, M. & Cook, P.W. 2000, "Power-aware microarchitecture: design and modeling challenges for next-generation microprocessors", Micro, IEEE, vol. 20, no. 6, pp. 26-44.
- [15]. Patterson, D. 2010, "The trouble with multi-core", Spectrum, IEEE, vol. 47, no. 7, pp. 28-32, 53.
- [16]. Intel Corp., "Intel core i7-940 processor," Intel Product Information, 2009 [Online]. Available: http://ark.intel.com/cpu.aspx.
- [17]. D. Geer, "Chip Makers Turn to Multicore Processors," Computer, vol. 38, pp. 11-13, 05, 2005.
- [18]. Blake, G., Dreslinski, R.G. & Mudge, T. 2009, "A survey of multicore processors", Signal Processing Magazine, IEEE, vol. 26, no. 6, pp. 26-37.
- [19]. J. Yan and W. Zhang. "Hybrid multicore architecture for boosting single-threaded performance", In ACM SIGARCH Computer Architecture News, Vol 35, No.1, pp. 141-148, March, 2007.
- [20]. International Journal of Engineering and Technology Volume 2 No. 5, May, 2012 by A.I. Fasiku, JB Olawale, O.T. Jinadu.
- [21]. Xinmin Tian, M. Girkar, S. Shah, D. Armstrong, E. Su and P. Petersen, "Compiler and runtime support for running OpenMP programs on pentium- and itanium-architectures," in High-Level Parallel Programming Models and Supportive Environments, 2003. Proceedings. Eighth International Workshop on, 2003, pp. 47-55
- [22]. Jongman Kim, Dongkook Park, Theocharides, T., Vijaykrishnan, N. & Das, C.R. 2005, "A low latency router supporting adaptivity for on-chip interconnects", Design Automation Conference, 2005. Proceedings. 42nd, pp. 559
- [23]. Y. Hoskote, S. Vangal, A. Singh, N. Borkar and S. Borkar, "A 5-GHz Mesh Interconnect for a Teraflops Processor," Micro, IEEE, vol. 27, pp. 51-61, 2007.
- [24]. Moore, S.K. 2008, "Multicore is bad news for supercomputers", Spectrum, IEEE, vol. 45, no. 11, pp. 15-15.
- [25]. Multi-core processor review by Balaji Venu department of electrical and electronic engineering university of Liverpul, UK.
- [26]. A. I. Fasiku, (2012); Performance Evaluation of Multicore Processors, M.Tech Thesis, Federal University of Technology, Akure, Nigeria.
- [27]. "Multi-core architecture" presentation by Jernej Barbic 15-213, spring 2007 May3, 2007.

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