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Hardware implementation of modified pseudo chaotic sequence generator for DS_SS communication system

Neetha. G[1], Kavitha. V[2]
[1]M. Tech., CMRIT Bangalore, India
[2]Ph.D Scholar, Jain University, India

Abstract: Direct sequence spread spectrum technology (DS-SS) is the most commonly used technology for code division multiple access. It is designed to overcome the interference problems associated with narrow-band very high frequency data transfer systems. Spread spectrum communication is used to reduce jamming of communication and provides a heightened secure communication. In this paper we specifies the design and Field Programmable Gate Array (FPGA) implementation of a direct sequence spread spectrum communication system using modified pseudo-chaotic sequences (PCS) for spreading digital data. Here pseudo-chaotic sequence generator used is the Universal asynchronous linear feedback shift register (UALFSR). The sequence generator and the Direct Sequence Spread Spectrum (DS-SS) system are implemented on FPGA. The generated pseudo-chaotic sequences are highly random in nature, suitable for highly secure communication and DS-SS communication with large number of users. Performance of the system is evaluated and it reveals that the DS-SS system using PCS sequences generated by UALFSR significantly outperforms the other chaotic sequences such as sequences generated by non linear feedback shift register (NLFSR).

Keywords: Digital communication, spread spectrum, pseudo-noise, chaos, chaotic sequence generator.

1. Introduction

Spread spectrum (SS) has been defined as a means of transmission in which the signal occupies bandwidth much in excess of the minimum necessary to send the information. The band spread is accomplished by utilizing a code which is independent of data and a synchronized reception with the code at the receiver is used for de-spreading and subsequent data recovery. There are many types of spread spectrum techniques such as Direst sequence (DS), frequency hopping, time hopping and hybrid system. Performance of Direct sequence technique is usually more reliable than the other techniques so we are considering DS_SS system in this paper.

Spread spectrum techniques for digital communication were originally developed for military application because of their high security and their susceptibility to interference from other interceptor. Now a day this technique is also used in variety of commercial application such as mobile and wireless communication.

Initially in order to spread the bandwidth of the transmitting signals, the binary pseudo-noise (PN) sequences have been used extensively. One of the commonly used PN sequence in DS-SS communication is maximal length sequences (m-sequences) [5]. The length of m-sequences depends on the number of shift register. Good correlation can be achieved with m-sequences but this sequence has many disadvantages – Transmission is not completely secured [7]. The number of sequences generated by LFSR may be insufficient for wide band DS-SS with a very large number of users. It provides limited flexibility in incorporating security into multiple user systems [6].

In order to overcome the disadvantage of PN sequences, the chaotic sequence has been proposed .It is sensitive to initial conditions and has a characteristic similar to random noise. Nonlinear feedback shift register (NLFSR) can be used to generate the chaotic sequence but in this user has no control over the generated sequence. In order to make it universal and user controllable generator, PCS sequence that uses universal asynchronous linear feedback shift register is proposed. This is applicable for all polynomial and has better device utilization and timing summary than the PCS generator which uses NLFSR.

2. Related work

Pseudo noise (PN) is defined as a coded sequence of 1's and 0's with certain auto-correlation properties [4]. The system of sequences used in spread spectrum communication is usually periodic in that a sequence of 1's and 0's repeats. The m-sequence represents a commonly used periodic PN sequence [5].

Such sequences are long periods and require simple instrumentation in the form of a LFSR. A shift register of length m consists of m flip-flops (two state memory stages) regulated by a single timing clock. In a feedback shift register of the linear type, the feedback function is obtained using modulo-2 addition (XORed) of the outputs of the various flips-flops. The generated m-sequence is always periodic with a period of N=2m-1 where 'm' indicates is the length of the shift register. Circuit required will be more for long periodicity sequence. The PCS Generator generates a pseudo-chaotic sequence with good cross correlation and auto-correlation properties that is well suited for DS-SS system. Because of long periodicity, it provides very high security and is capable of handling many users.

3. PCS Generator

A. Generation of Pseudo chaotic sequences.

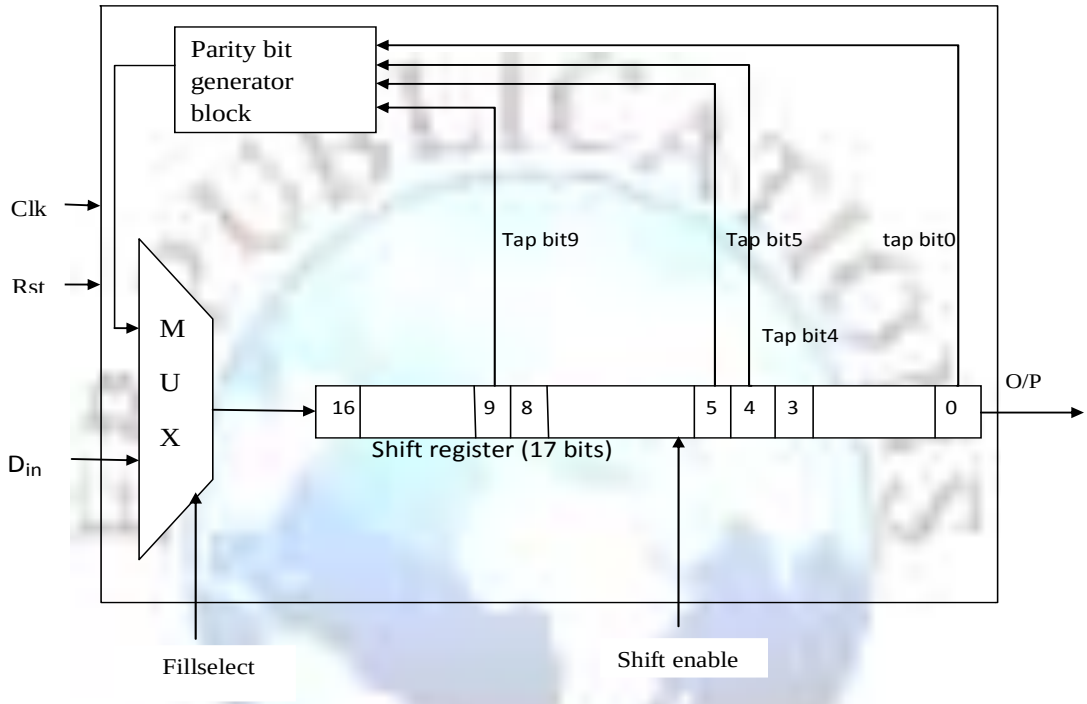

Fig 1: Block diagram of UALFSR

Block diagram of Universal asynchronous linear feedback shift register is shown in the figure1. It consists of shift register which has 4 tap points and whose width is 17, 2:1 multiplexer and parity bit generator block. It has Clock, Reset, single bit data input, fill select, shift enable signals as input and output is the LSB bit of shift register.

If Fill select =1, D_{in} is the output of MUX else if Fill select =0, parity bit is the output of MUX. Four tap points namely bit0, bit4, bit5 and bit9 are taken from shift register and given as inputs to the parity generator bock. XOR operation is performed on the tap bits to generate parity bit which is given as one of the input to the MUX. When input reset signal 'RST' is high, all bits of shift register are logic zero and therefore output is also logic zero. When 'RST' signal is low and shift enable is high, right shifting is performed on shift register by shifting one bit position. During right shifting, output of MUX is loaded to the MSB bit position of shift register and LSB bit which is shifted out from the register will be the output of sequence generator.

B. Flowchart of UALFSR

Flowchart of UALFSR is shown in the figure2. After starting, it will check the fill select signal for logic high condition. If the condition is true output of the MUX is the user given data input. If the condition is false then parity bit which is generated by performing XOR operation on tap bit will be the output of MUX. Next it will check for reset signal for logic high condition If it is true all the bits of shift register will be zero and output is also zero otherwise it will check the shift enable signal for logic high condition. If it is true right shift operation is performed otherwise shifting operation is not performed. Output is the LSB bit of shift register.

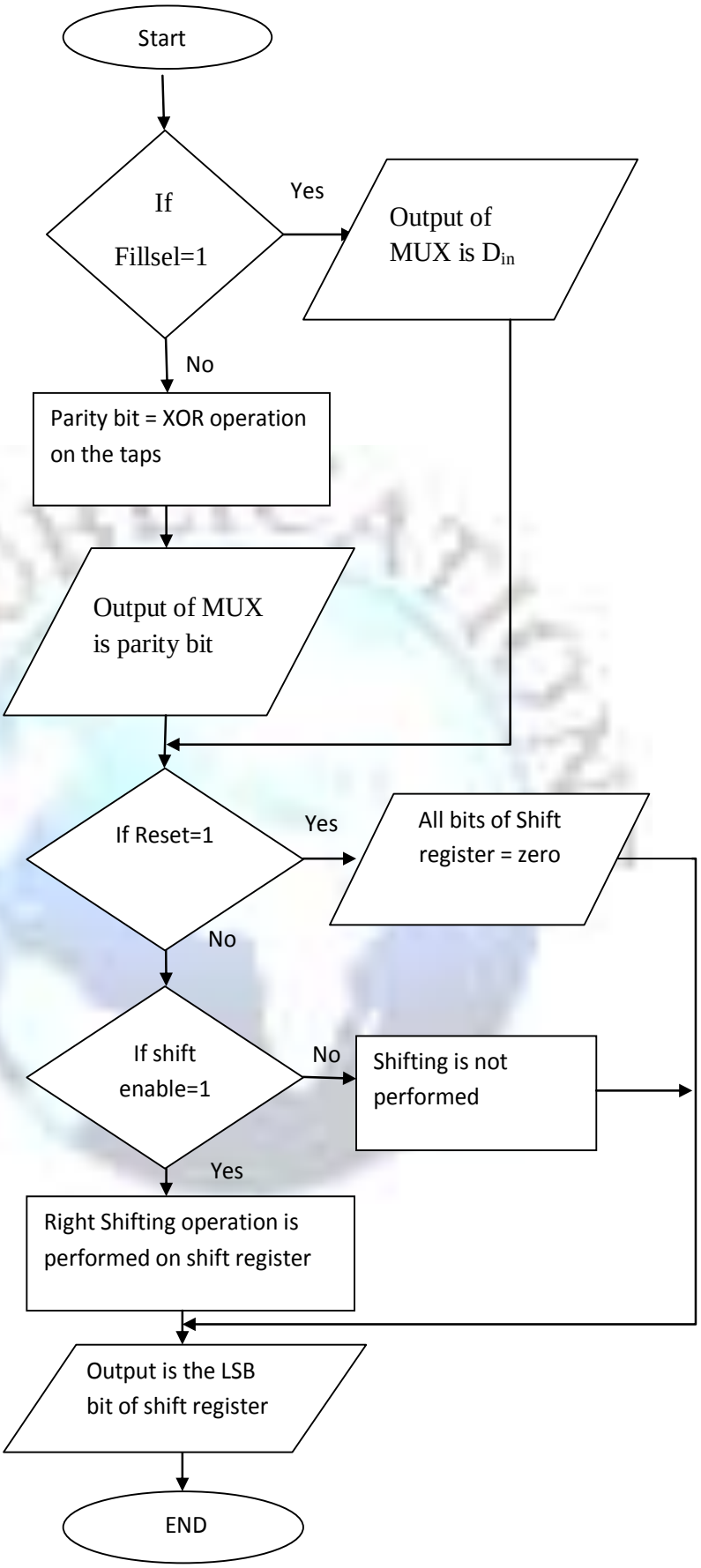

Fig 2: Flowchart of UALFSR

3. Transmitter

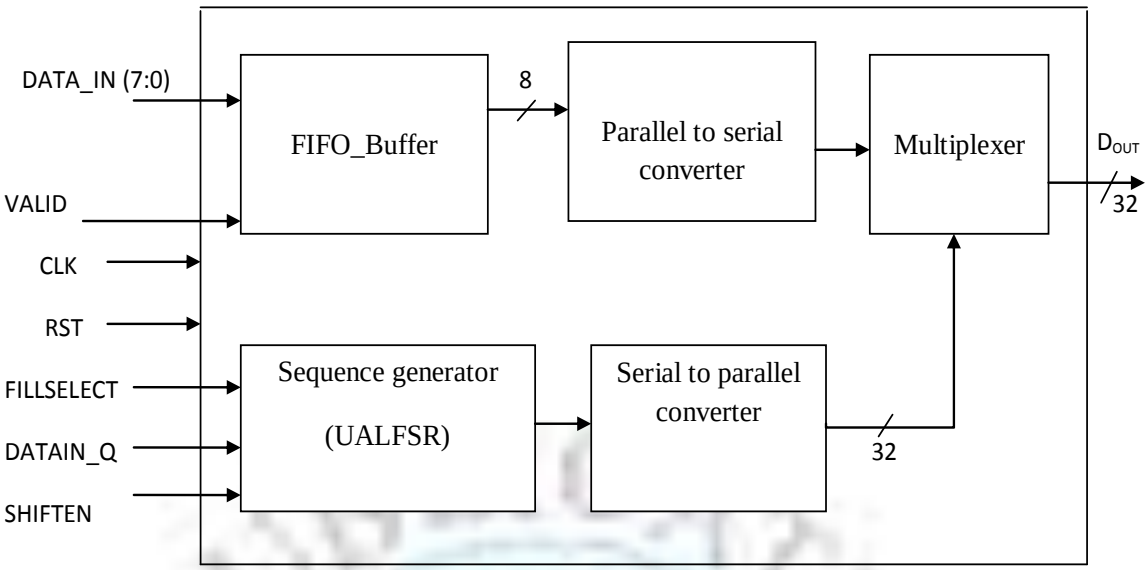

Fig 3: Block diagram of Transmitter.

Block diagram of Transmitter designed in this project is shown in the figure3. It consists of sequence generator (UALFSR), Buffer (FIFO), Parallel to serial converter, multiplexer and serial to parallel converter. The input signals given to the transmitter are input data which is of 8 bits, clock, reset, valid, fill select, single bit data and shift enable and output is spreaded data which is of 32 bits.

The main function of the transmitter is to spread the information data using pseudo chaotic sequences which is independent of the data. When clock is given, reset=0 and if the input signal 'valid' is logic one then data which is to be transmitted is stored into the buffer. The output of buffer is given as input to the parallel to serial converter when output signal 'rd' becomes high. Sequence generator, based on the value of fill select takes either user given data or feedback data and generates random sequences. These sequences are given as input to the serial to parallel converter which outputs parallel data of 32 bits. Output of parallel to serial converter is given as a select line for the MUX. If it is high then 32 bit parallel_data_out (spreaded data) is the output of transmitter otherwise output of transmitter will be zero (32bits).

Therefore spreaded data (transmitted data) is obtained by multiplying each bit of information data with 32 bit chaotic sequences. The bandwidth expansion factor which is also called as processing gain (K) is defined as the ratio between the transmitted spread spectrum signal bandwidth (B) and the bandwidth of the original data sequence (B message). Processing gain is nearly the ratio of spread bandwidth to the information rate R (bits/s) and it is much greater than unity.

$$K = \frac{B}{B_{message}} \approx \frac{B}{R}$$

4. Receiver

Block diagram of receiver designed in this project is shown in the figure 4. It consists of sequence generator, two serial to parallel converter blocks and bit correlator. Input and output signals of the receiver are shown in the block diagram. Main function of the receiver is to despread the received data using same pseudo chaotic sequences which is used during transmission to generate original information data.When clock is given and reset is set as low, sequence generator will generate the spreading sequences. These sequences are given as input for the serial to parallel converter (1). This converter takes serial data and outputs 32bits parallel data.
This parallel data is given as input for the correlator. Correlator has another input i.e.32 bit transmitted data. In this XOR operation is performed on the inputs and gives single bit data as output. This data is given to the serial to parallel converter (2). This converter outputs the original information data 'DATA_OUT' which is of 8 bit.

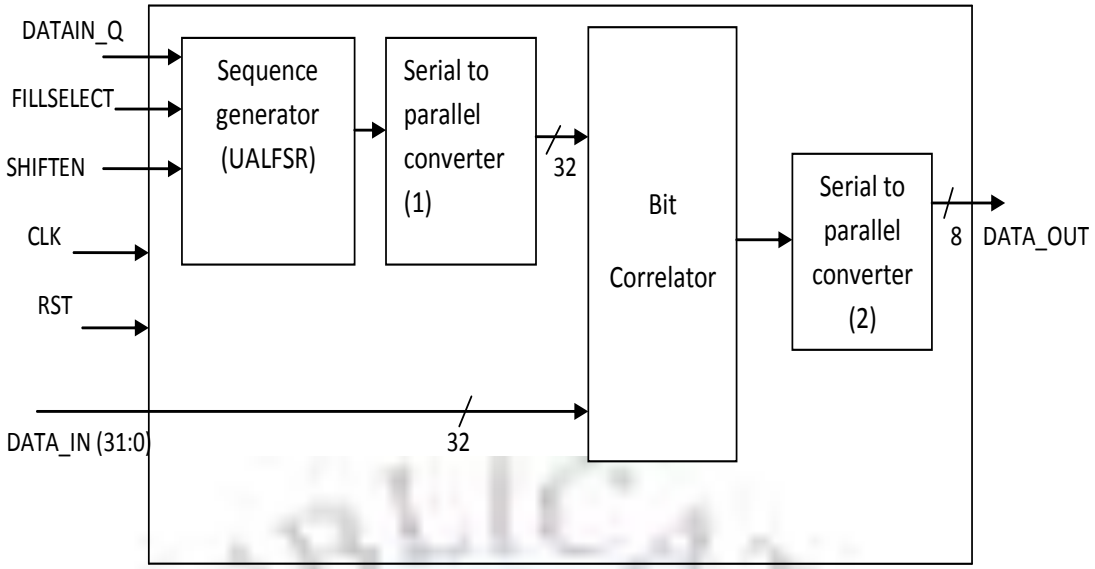

Fig 4: Block diagram of Receiver.

5. DS_SS system

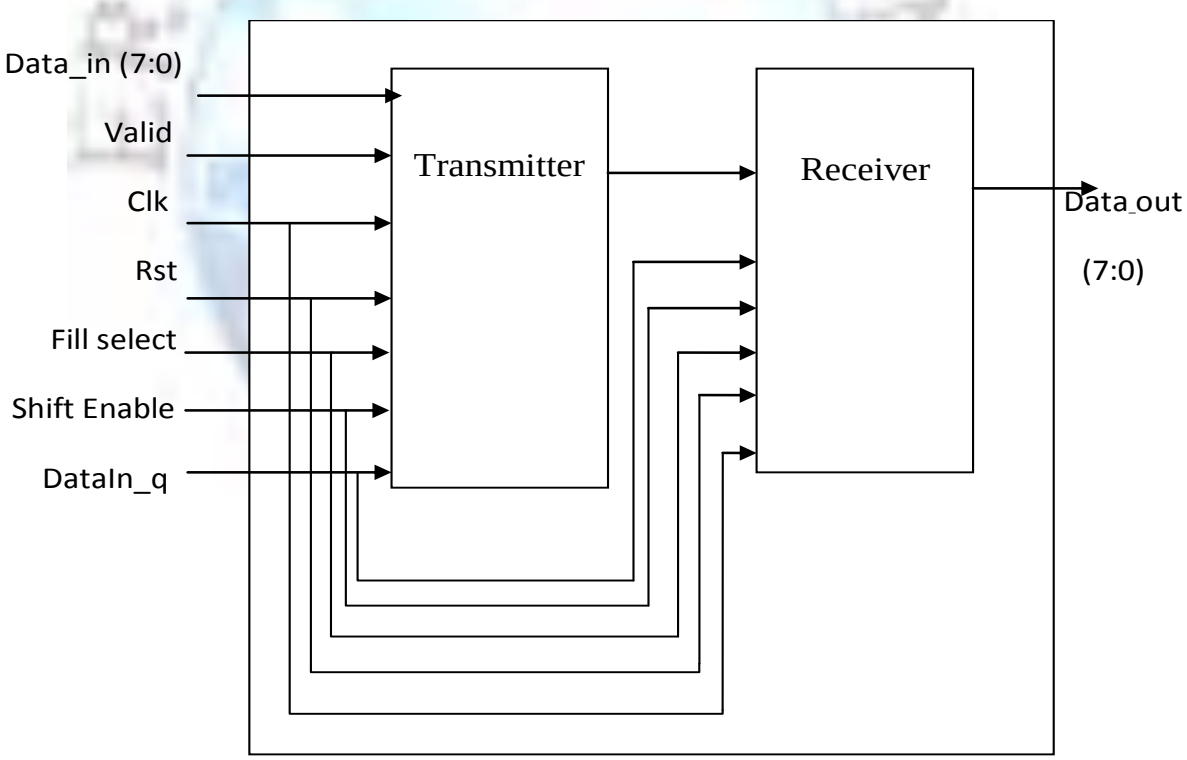

Fig 5: Block diagram of DS_SS system

Block diagram of DS_SS system and its input and output signals are shown in the figure 5. Direct sequence spread spectrum communication system multiplies the data being transmitted by a "noise" signal. The noise signal is a binary pseudo chaotic sequence, at a frequency much higher than that of the original signal. This process is called "spreading". The resulting signal resembles white noise. However, this noise-like signal is used reconstruct the original data at the receiving end, by multiplying it by the same binary pseudo chaotic sequence. This process is known as "de-spreading". The designed DS_SS system is implemented on FPGA Spartan 3 board.

6. Results

A. Simulation Result

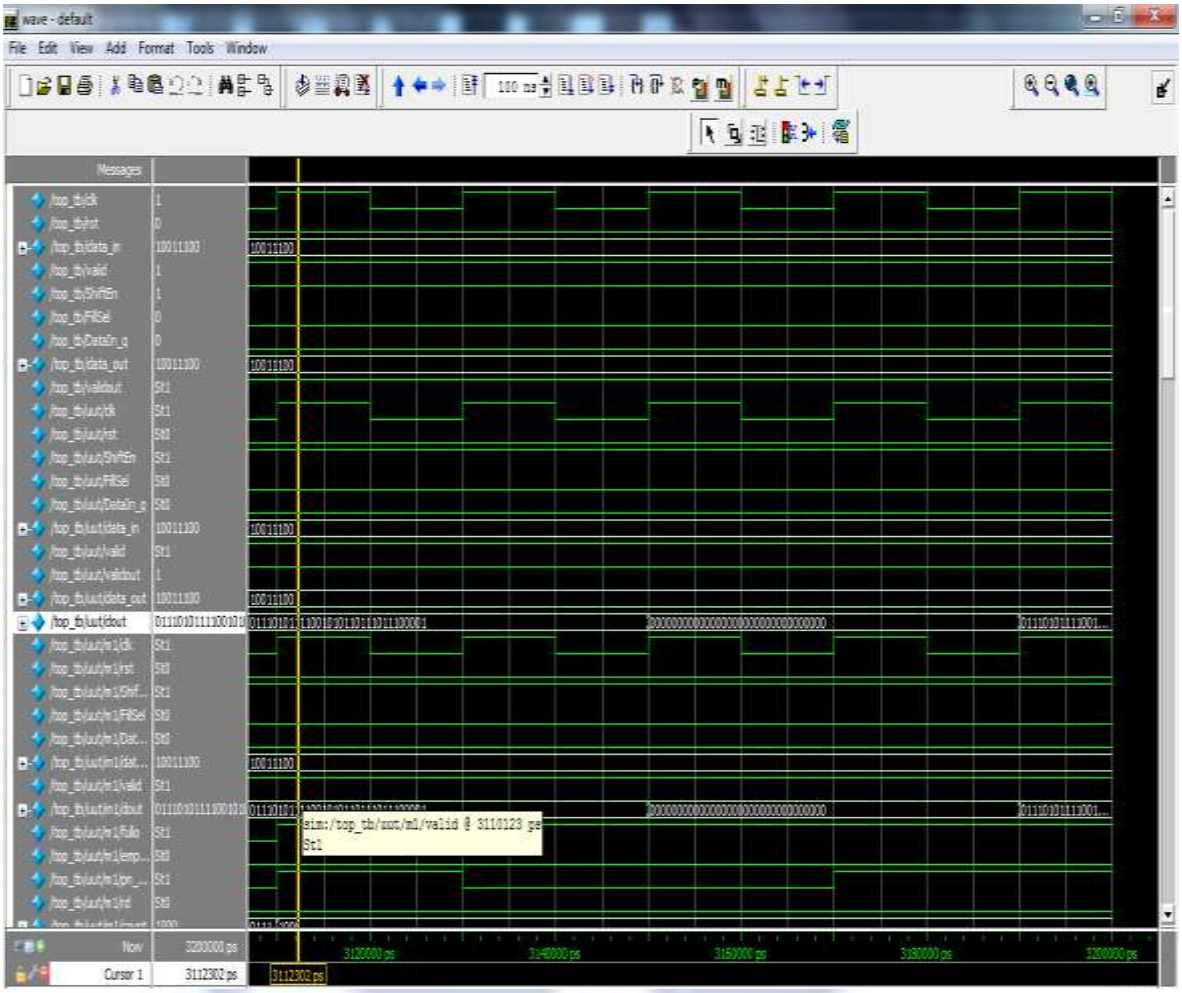

Fig 6: Simulation results of DS_SS system

Above figure shows the simulation result for direct sequence spread spectrum communication system when clock is given, reset is set as low. Valid and shift enable inputs are set as logic one and Fill select and DataIn_q inputs as logic zero. The input information data (8bit) given is 10011100 and output is the recovered information data (data_out) at the receiver which is shown in the figure.

B. Device utilization

Logic Utilization	Utilization	
	DS_SS system (Using NLFSR)	DS_SS system (using UALFSR)
Number of slices	33%	4%
Number of slice Flip Flops	20%	2%
Number of 4 input LUTs	19%	3%
Number of bonded IOBs	27%	16%
Number of GCLs	25%	12%

Table 1: Device utilization summary of PCS based DS_SS systems

C. Timing summary

	DS_SS system using NLFSR	DS_SS system using UALFSR
Speed Grade	-5	-5
Minimum period	15.417ns	12.178ns
Maximum frequency	64.863MHz	82.113MHz
Minimum input arrival time after clock	27.168ns	6.056ns
Maximum output required time after clock	23.911ns	6.141ns

Table 2: Timing summary of PCS based DS_SS systems

Conclusion

In this dissertation, we have designed and implemented a modified pseudo chaotic sequence (PCS) generator and direct sequence spread spectrum (DS_SS) communication system using this modified PCS generator. Here Universal asynchronous linear feedback shift register (UALFSR) is implemented instead of nonlinear feedback shift register (NLFSR) to generate pseudo chaotic sequences. The sequence generated will be random in nature hence suitable for secure communication. Since length of the sequence is long it is also suitable for multiple user system and it overcomes the interference problem associated with narrowband high frequency data transfer system. Implemented generator is applicable for all polynomials and user has the control over generated sequence. The PCS based Transmitter and receiver of DS_SS system is also designed and implemented.

Performance of the system is evaluated and by analyzing device utilization and timing summary it reveals that the DS-SS system using PCS sequences generated by UALFSR significantly outperforms the other chaotic sequences such as sequences generated by NLFSR. Device utilization summary and timing report for PCS generator and PCS based DS_SS system is shown in the chapter 6. For PCS based DS_SS system maximum device utilization is about 16% and maximum frequency is 82.113MHz.

Acknowledgment

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References

[1]. DS-SS communication system using pseudo chaotic sequences generator in 2013
[2]. Lathi-1998] Lathi, B.P. Modern Digital and Analog Communications Systems. 3rd Edition. New York: Oxford University Press.
[3]. Haykin-2001] Haykin, S. Communication Systems. 4th Edition. New York: John Wiley and Sons.
[4]. Bernard Sklar: Digital communication. Fundamentals and Applications. Prentice Hall. (2001).
[5]. G.Heidari-Bateni, C.D.McGillem: Chaotic sequences for spread spectrum: An alternative to PN-sequences. Proc. IEEE ICWC-92 437C440(1992).
[6]. D. Leon, S.Balkir,M.W.Hoffman, l. C. Perez:Pseudo-chaotic PN sequence generators circuits for SS communication. Proc. of IEECircuits Dev. Syst.151(6):543-550(2004).
[7]. Y. Soobul, K.Chady, Harry C.S Rughoopath: Digital chaotic coding and modulation in CDMA. Proc. of IEEE Africon 841-846 (2002).
[8]. Bob X. LI, Simon Haykin:A new pseudo-noise generator for spread spectrum communication. Proc. Of IEEE. 3603-3606(1995).
[9]. M. I. Youssef, M. Zahara, A. E. Emam, and M. Abd ElGhany: INTERNATIONAL JOURNAL OF COMMUNICATION issue2, volume2, 2008,chaotic sequence implementation on residue number spread spectrum system.
[10]. Ajeesh P. Kurian, Sadasivan Puthusserypady, Su Myat Htut: Performance enhancement of DS/CDMA system using chaotic complex spreading sequence. IEEE Trans. On Wireless communication. 4(3): 984- 989(2005).