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Performance of Low-Power Rail-to-Rail Operational Amplifier at Constant gm

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Abstract: A low power CMOS op-amp rail to rail op-amp. We realize in SCNO 180nm technology Under 1.8 power supply voltage. A constant Transconductance is ensured for the whole common-mode input range. The class AB output stage also has a full voltage swing. The circuit provides a gain bandwidth of 17.3-MHz and a DC gain of 83.67 dB. The input transistors operate in weak inversion, which have big gm/Id value, so the power consumption is reduced.

Keywords: CMOS, SCNO, DC, 173-MHz.

INTRODUCTION

With the development of wireless communication from the second generation (2G) to 3G, many communication standards, such as GSM, TD-SCDMA, WCDMA and CDMA2000 will co-exist for a long time. This phenomenon will also happen in navigation and broadcast television, as there are also many standards, for example: GPS, Galileo, CMMB, DVB-H and so on. So, the reconfigurable radio frequency integrated circuit (RFIC) and broadband data conversion circuit facing multi-standard and multimode wireless communication is very important. For the key part of this circuit, i.e. the RF front-end transceiver, the often taken structure is the zero-intermediate frequency scheme, as there is no image-rejection problem, and consumes less power. The operational amplifier (Op-amp) we proposed is suppose to be used between the down converter and the second stage ADC in the receiver end, and between DAC and the up-converter in the transmitting end. As the Op-amp has both input and output dynamic range rail-to-rail, we can lower requirement for ADC and DAC, thus to improve system performance. Also, battery powered device for communication such as cell phones drives IC to the low power. In this case, designing low-power That is, rail-to-rail. To ensure this, the minimum supply voltage should be Op-amp becomes the fundamental job of designing low-power analog and mixed signal systems. To reach the rail-to-rail amplitude, the input stage and the output stage should be designed respectively.[1]

We can optimize the input stage constant-g_m operation controlling of the total input current. In fact, as we know, in bipolar process and in MOS weak inversion, the g_m is proportional to the current, while in MOS strong inversion it is proportional to the square root of the current..For the high supply voltage, there are some ways to make $g_{m\ constant}$ of the often used ways is 1:3 current mirror. Our main goal is to realize a constant g_m input stage and a rail-to-rail output stage for a low-power operational amplifier.[2] This has been achieved by the current-switch transcondutance control circuit in the input stage and the improved class AB in the output one. The paper is organized as follows. The input and the output part will be introduced and analyzed the results are verified.

IMPLEMENTATION OF RAIL TO RAIL OP-AMP

The op-amp consists of three stages:

- Complementary input stage with constant gm circuitry
- Folded cascade summing stage
- Class AB output stage

Analysis of Complementary Input Stage

Since the gm of a MOS transistor operating in strong inversion is proportional to the square-root of its drain current, the tail current of the actual active input pair could be increased by a factor of four [4]. This principle is realized in the circuit as shown in Fig.1. The g_m-control implemented by means of two current switches, m3n and m5p, and two current mirrors,

m3p – m4p and m5n – m4n each with a gain of three. The principles of the gm control can be best understood by dividing the common-mode input range in to three parts. If low common-mode input voltages are applied, only the P-channel input pair operates. The N-channel current switch conducts while the P-channel one is off. The N-channel current switch takes away the reference current Isn and directs it to the current mirror, m3p-m4p, where it is multiplied by a factor three and added to Isp. Since Isp and Isn are equal, the tail-current of the P-channel input equals 4Isn.If intermediate common-mode input voltages are applied, the P-channel as well as the-n channel input pair operates.[3] Now, both current switches are off. The result is that the tail currents of the N-channel input pair and that of the P-channel input pair are equal to I_{SN} or Isp. If high common-mode input voltages are applied only the N-channel input pair operates. The P-channel current switch conducts while the N-channel current switch is off. The P-channel current switch takes away the current Isp and feeds it into the current mirror, m4n-m5n, here it is multiplied by a factor 3 and added to the current Isn. The result is that the tail-current of the N-channel input pair equals

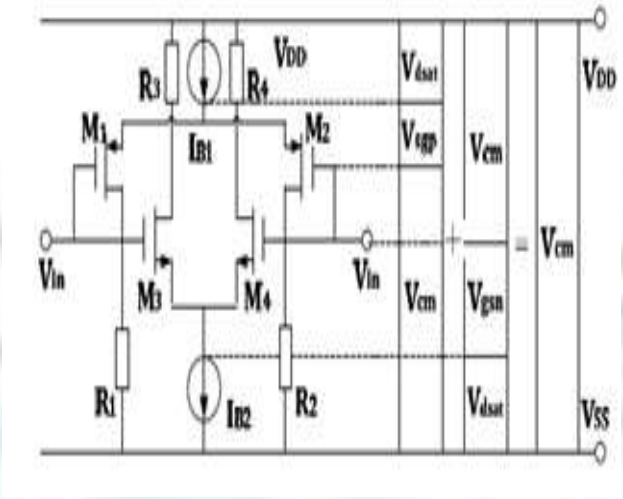

Figure 1. The input range of

Complementary differential pair

By placing two complementary differential pairs in parallel as shown in Fig. 1, it is possible to obtain a rail-to-rail input stage. The NMOS pair is conduction for high input common-mode voltages, in particular

If $V_{SS}+V_{gsn}\ V_{dsa\,t} < V$common)
While the pMOS pair is in conduction for low input common-mode voltages
$Vc_{ommon} < V_{DD}-V_{dsat}-V_{sgp}$

When both pair are in parallel,the input dynamic range can be
$V_{ss}<V_{Common}<V_{DD}$
That is, rail-to-rail. To ensure this, the minimum supply voltage should be

Vsupmin=Vsgp+Vgsn+Vdsatn+Vdsatp

However, a main shortcoming of a rail-to-rail structure is that its total transconductance will change. That is, when the input voltage can make both pairs on, its total transconductance will be twice of that when only either pair is on. This will bring to the change of the loop gain and thus cause distortion. What's worse? It will decrease phase margin and make the Op-amp unstable As the transistors in the proposed circuit work in weak inversion, their trans conductance are proportional to the currents in them

$$\mathbf{g_{miweak}=I_p/2n_pV_T+I_n/2n_nV_T}$$

Where, Ip and In are the current in the PMOS and NMOS pair, np and n_n are slope factors of the weak inversions. V_T is the thermal voltage. So, to make gm constant, we can tune the current within the input range

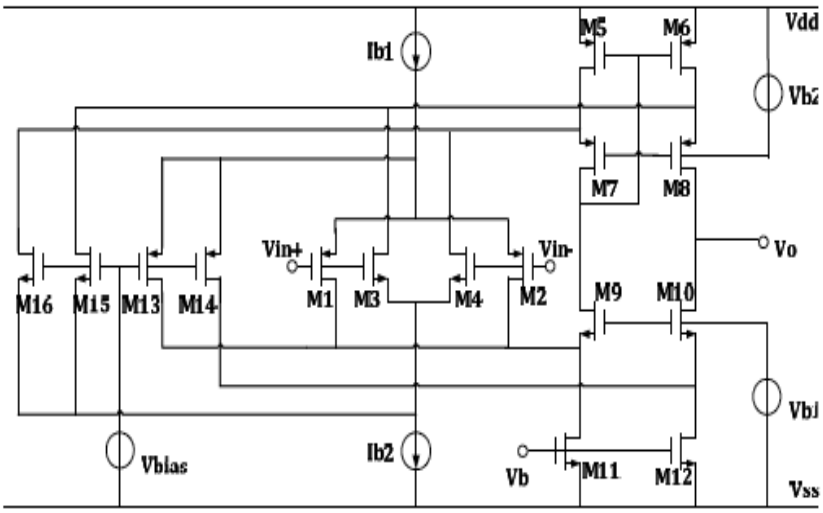

Figure.2. Current switch transconductance control circuit

As can be seen from Equations, and Fig.2, we set V_{bias} voltage to be 0.9 V. When the input voltage is low enough, pMOS differential pair M1 and M2 are on while NMOS Differential pair M3 and M4 are off. Then, Ib1 will come through M1 and M2, Ib2 will come through M15 and M16, and so the total gm will be

gm=gmp=Ip/2npV.

When the input voltage is high enough, NMOS transistorsM3 and M4 are on while PMOS transistors M1 and M2 are off.Ib1 will pass through M13 and M14 while Ib2 though M3 andM4, thus the total gm will be

gm=gmn=In/2nnVT

When the input voltage is in the middle range, both pairs are on, the current switch M13, M14, M15, M16 will take away some of the current from Ib1 and Ib2, thus the total gm will be

gm=gmp+gmn=Ip/2npVT+In/2nnVT

Suppose the input voltage is 0.9 V, here M1~M4 will take 1/4 of the tail current, the expression will be

gm = Ip/4npVT + In/4nnVT

To have gm constant, we should modify transistor size to Make

Ip/np=In/nn

Here the input stage delivers a constant output current to the summing circuit, which consist a high-swing current mirror (M5-M8) and common-gate stage (M9,M10). Gain can be improved by raising the tail current, however, to make sure input transistors are in weak inversion, the width and length of input transistors should be improved which at the same time can lower the offset of the circuit.

Cascode Summing Stage

The amplifier uses a folded-cascode current-summing gain stage output branches to provide output voltage for the class AB output stage[7]. The gain stage consists of PMOS cascade transistors M4, M8 and NMOS cascade transistors M5, M9 along with PMOS current sources M3, M7 and NMOS current sources M6, M10.Output stage of class AB op-amp show in fig 3.

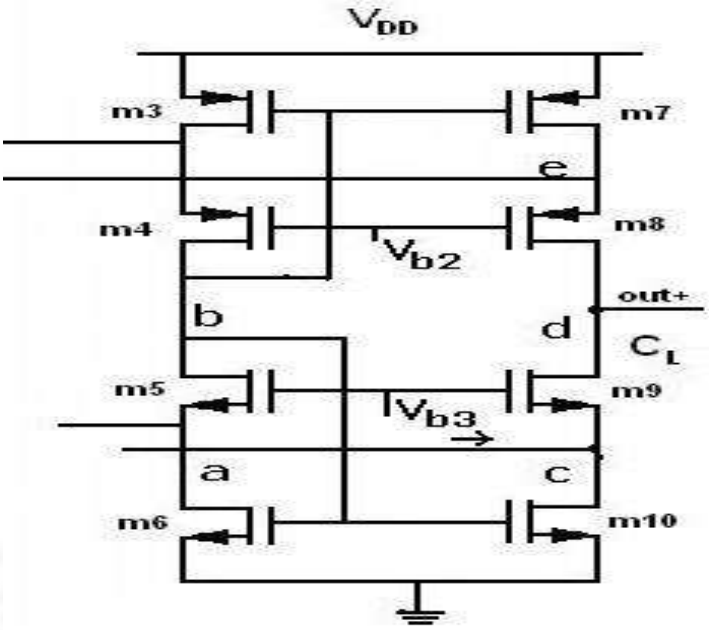

Figure-3. Output stage of class AB op-amp

CLASS AB OUTPUT STAGE

To make efficient use of the supply voltage and supply current, an op-amp requires class-AB biased output transistors connected in a common-source configuration. Moreover, the class-AB control should be compact to efficiently use die area .The floating class-AB control transistors, the stacked diode connected transistors and the output transistors set up two Trans linear loops m13, m14, m11, m17and m12, m15, m16, m18, which determine the quiescent current in the output transistors.[6] The class-AB action is performed by keeping the voltage between the gates of the output transistors constant. The current of the P-channel class-AB transistor, M11, increases while the current in the N-channel class-AB transistors, M12, decreases by the same amount. Consequently, the gate-voltages of both the output transistors move up. Thus the output stage pulls a current from the output node. The current of the P-channel output transistor is kept at a minimum value, which can be set by W over L ratios of the class-AB control transistor . M27 and M28 are the output part. M19 and M20 form a class AB control circuit points A and B have a small DC voltage, which can make sure that outpu transistors will not both be off thus to avoid cross-over distortion.

$$V_{gs19}+V_{gs27}=V_{gs22}+V_{gs23}$$

$$V_{gs20}+V_{gs28}=V_{gs25}+V_{gs26}$$

quiescent current

$$Iq = \frac{W/L27}{W/L23} I21$$

Here we suppose the currents in M21 and M24 are the same, and the following equation is satisfied

$$\frac{(W/L)27}{(W/L)28} = \frac{(W/L)22}{(W/L)25} = \frac{(W/L)19}{(W/L)20}$$

To make the quiescent current stable, M29 and M30 were added as floating current source, so as to bias the class AB control circuit. Here M29 and M30 has two parts to play, one is

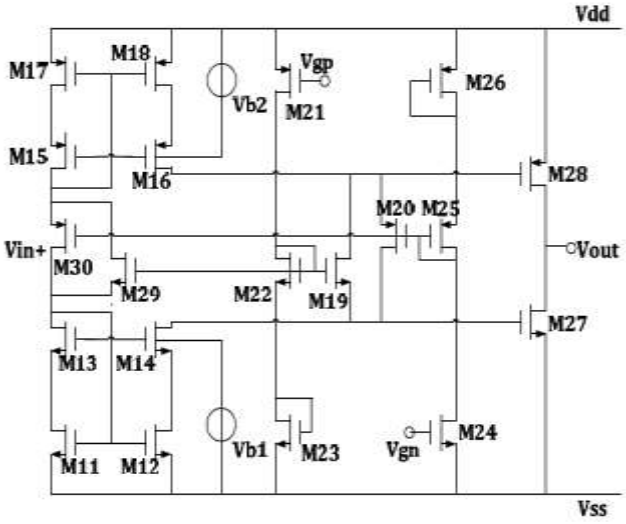

Figure.4 The improved output structure

with floating current source to compensate the effect of voltage source, as they are the same structure of M19 and M20. In this way, PSRR of the circuit can be improved. The second is to make the quiescent current stable, less affected by the common mode input voltage The whole circuit can be seen in Fig. 3.12. We see that the cascaded Miller frequency compensation method was used. Compared to the classical Miller compensation, this method shifts the non-dominant pole to higher frequency

OVERALL CIRCUIT DESIGN

A compact op amp with Miller compensation has been designed, and is shown Fig.3 [5]. The overall circuit of op amp consists of the rail-to-rail input stage, m1n, m2n, m1p, m2p, gm-control, m3n-m5n and m3p-m5p , a summing circuit, m3-m12, and a rail-to-rail class- AB output stage, m17-m18.The floating current source, m21-m22,biases the summing circuit and the floating class-AB control.

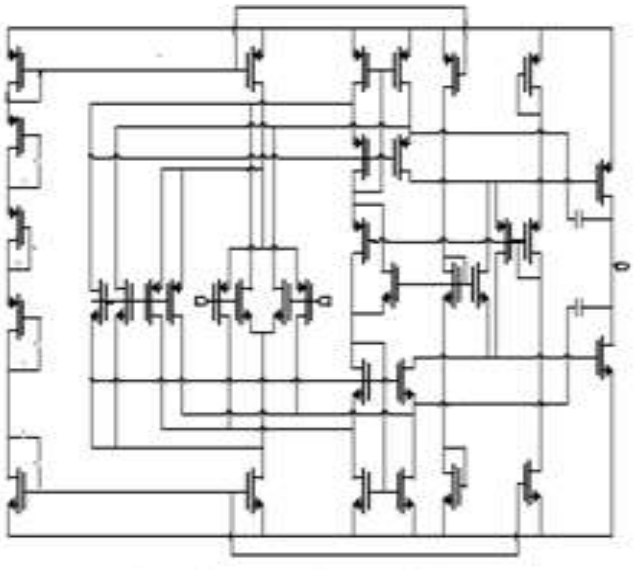

Figure: 5 The proposed op-amp circuit

The value of the current source is set by two trans linear loops, m13, m14, m3, m21and m6, m15, m16, m22. The mirrors, m3, m4, m7, m8 and m5, m6, m9, m10, are loaded by the drain currents of the input pairs m1n-m2n and m1p-m2p, respectively. These drain currents, and consequently the gate-source voltages of m3 and m6 change with the common-mode input voltage. If, for example, the common-mode input voltage approaches the positive supply rail, the gm control circuit

increases the current Isp and decreases Isn. As a result, the gate-source voltage of m3 decreases while the gate-source voltage of m6 increases. However, this hardly effects the value of the floating current source, m21-m22 because an increase of the gate-source voltage of one mirror compensates for a decrease in the other mirror.

SIMULATION RESULT

Simulation result of rail to rail op-amp using mosis fabrication library and electrical specification of CMOS op-amp show in table 1 in load capacitance 5 pf and supply voltage 1.8 volt .table 4.2 show process parameters**.**

Table 1 PROCESS PARAMETERS (SCNO180 nm Tech.)

$\mu C_{ox}/2$: NMOS (A/V^2)	173.9
$\mu C_{ox}/2$: PMOS (A/V^2)	35.0
Vthpmin (volt)	0.37
Vthmax(volt) NMOS	0.50
ICMR(Volt)	1.3
Vdd(volt)	1.8

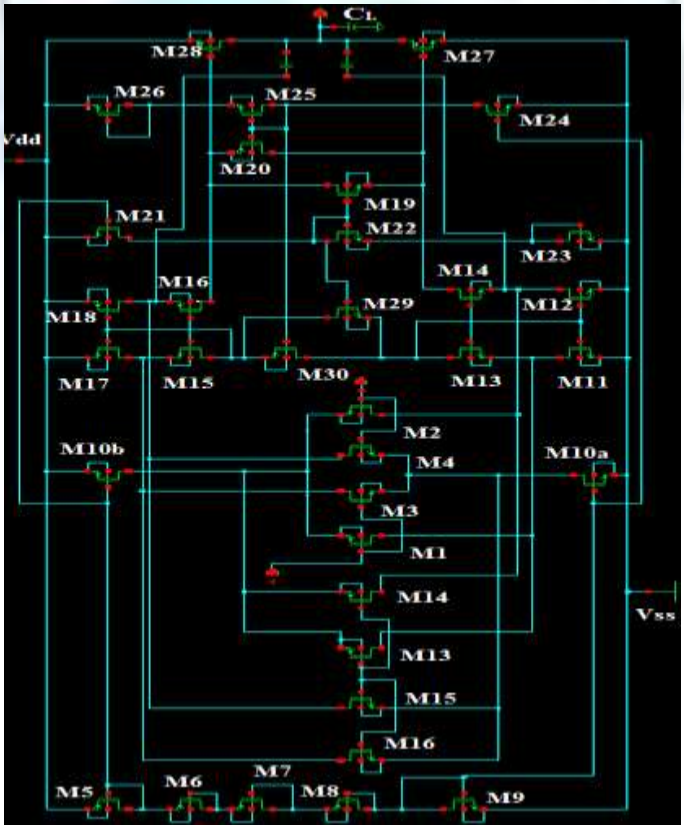

Figure 6-Overall circuit of rail to rail CMOS op-amp

AC Response

Through AC response we can simulate the schematic to find out the bode plot and phase plot. In Figure 3.7, a bode plot and phase plot for 1.8 V, 27° C and CL = 5 pf is shown. As can be seen, the open loop gain is 62.05 dB, and a phase margin is -13.69°. The unity gain bandwidth is 17.15MHz and f bandwidth is 1.74 KHz.

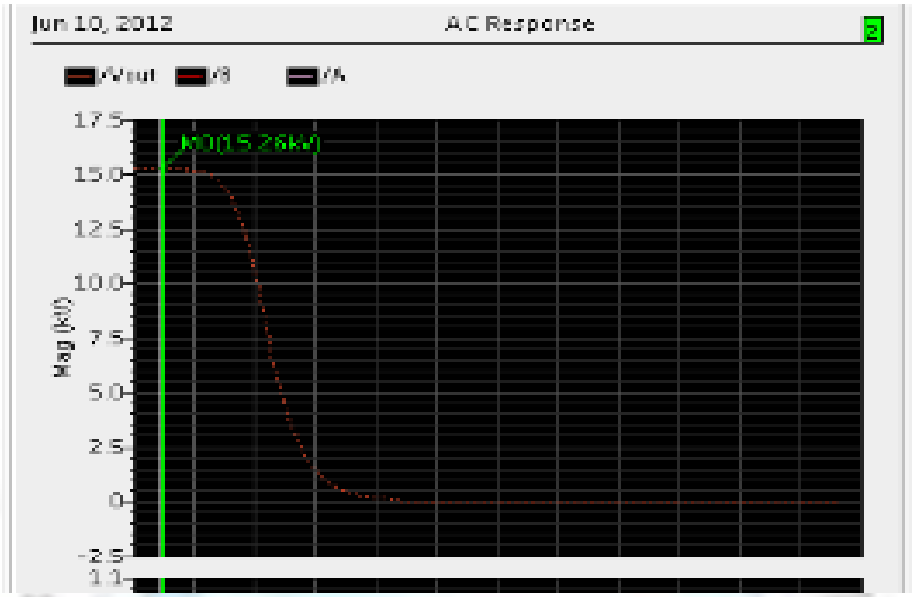

Figure 7-Chaterstic of AC response

Transient Step Response

In Figure 8, a step from ground to V_{DD} is applied at the input with unity feedback configuration. The slew rate of op-amp is 11.22 V/µS for rising edge of pulse and 11.10 V/ µS for falling edge of the pulse.

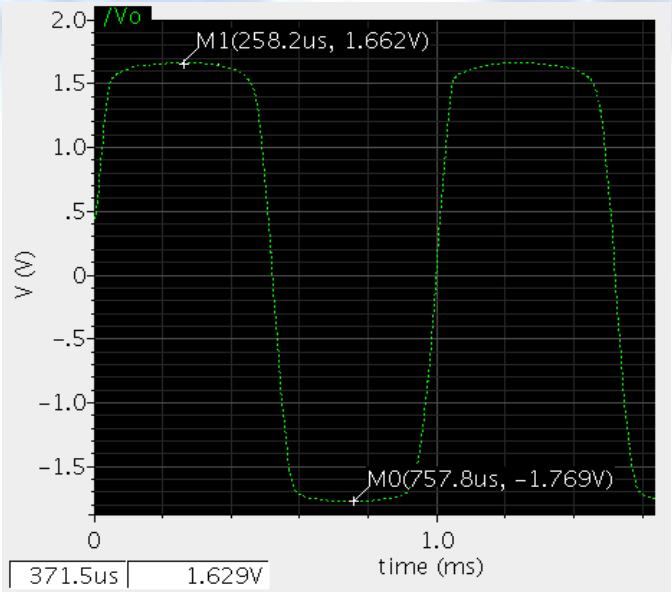

Figure 8 Chaterstic of transient step response

Gain And Phase

Gain and phase -Fig-6 and Fig-7 shows DC gain and Phase .its represent DC gain is 83.67db and phase 136 deg at vdd=1.8 and SCNO 180nm tech.

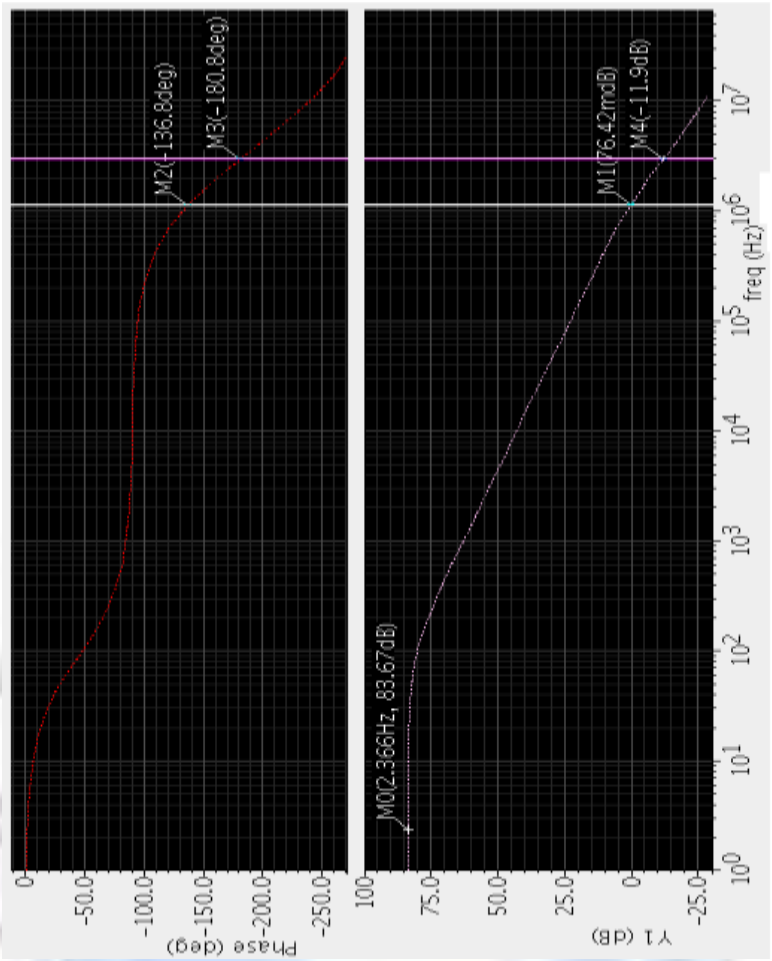

Figure 9- Chaterstic of Gain and Phase

GAIN MARGIN GM PHASE MARGIN PM OF OP-AMP-

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input The absolute value of the open-loop phase shift between the output and the inverting input at the frequency at which the modulus of the open-loop amplification is unity. Gain and phase margins are measures of stability for a feedback system, though often times only phase margin is used rather than both. Based the magnitude response of the loop gain

Gain margin is a measure of closeness of phase crossover point to (−1, j0). in GH plane. At phase crossover ωc, GH = G(jωc)H(jωc).

Gain margin = 20log10|G(jωc)H(jωc)|

is Usually positive. If gain is increased and |GH| goes through (−1, j0), the system has gone unstable. If GH never cuts negative axis the system is forever stable. Gain margin is the amount of gain in dB that can be allowed to increase in the loop before closed loop system reaches instability.

Phase Margin is how much to rotate the gain crossover point so that you go through (−1, j0).
Phase margin is defined as the angle in degrees through which the G(ω)H(ω) plot must be rotated about the origin in order that gain crossover point on locus passes through (−1, j0) point.
$\varphi M = 6\ GH - 180^0$

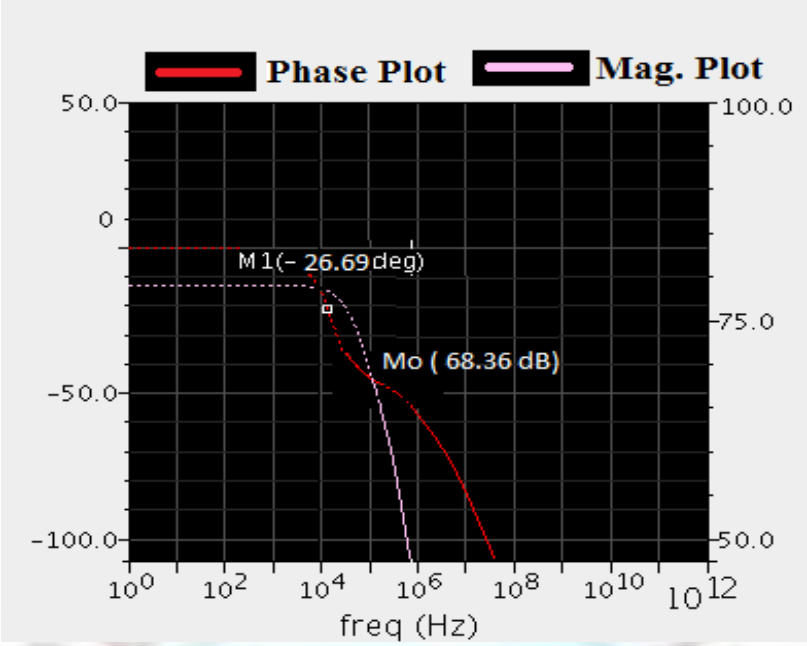

Figure 10 Chaterstic of gain and phase margin

Table 2: SIMULATION RESULTS OF RAIL TO RAIL OP-AMP (180nm Technology)

Specifications	**Theoretically value**	**Simulation results**
DC gain (dB)	**76**	83.67
GB (MHz)	17.3	17.9
Phase margin	-	153.3
Gain margin	-	68.6
CMRR (dB)	**178.8**	
ICMR (V)	1.3	1.0
Slew rate (V/µS)	10.8	11.2
Power dissipation(µW)	99.4	
I_{D5}(µA)	10.8	11.8
I_L(µA)	64.8	60.1
Load capacitance (pf)	5	5
Supply voltage (V)	1.8	1.8

CONCLUSION

We simulate the proposed Op-amp at 180 nm using **cadence virtuous** and measure the performance. By the proposed structure we got excellent result of dc gain and Slew rate. If it is less than the simulated one (not totally realistic, because technology dispersion are not taken into account) dc gain and GBW shows increase DC gain decrease GBW frequency. then I say that yet increase bandwidth of op-amp then balance DC Gain , good being to amplifier. if increase frequency then these amplifier work at oscillator .so we have to balance condition in both.

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