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Low Power Clock Gated Sequential Circuit Design

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ABSTRACT: Reducing Power dissipation is one of the crucial problems in today's scenario. So this dissipation has become a bottleneck in the design of high speed synchronous systems which are operating at high frequency. Clock signals have been a great source of Power. Design can be made on the basis of Clock gating approach to reduce the consumption of clock's signal switching power which is the foremost component for the utilisation of the power. The idea of clock gating is to shut down the clock of any component when it is not accessed. Clock gating avoids the redundant switching of clock signal. This Paper presents the design of clock gating technique based sequential circuit; D flip flop, Linear Feedback Shift Register , UART and estimation of Power with or without clock gating. Power analysis is carried out using XILINX X Power Analyser.

Index terms: Adaptive Clock Gating (ACG), Clock Gating, Linear Feedback Shift Register, Power Dissipation, Universal asynchronous receiver transmitter (UART).

1. INTRODUCTION

Now a days with the spread in the CMOS technology, a millions of transistors are placed on a single chip. Due to integration the transistors on the small area, has permit the fall in the delay and increase in the operating frequency. More are the transistors on the single chip more the power they will consume. The growth in the networking, [2] demands for efficient, high performance network routers Due to CMOS scaling process and popularity of mobile appliances leakage power dissipation has become a significant contributor of the total power. Hence power optimization has become an important issue. Designers go through several iterations to optimize power in order to achieve their power plans. This power should be optimized from the initial stage of the design. Sequential circuits in design of any component consumes significant power because of the clock signal which` consumes 45% of the total chip power and this power is expected to increase in the next generation. Power is directly proportion to voltage and the frequency of the clock as expressed below:

$P=CV^2F$.[3] Hence there is need to reduce this power. Clock Gating is the techniques which reduce the power consumption of the circuit but clock gating require additional hardware [4] to be built in the circuit. Hence power is optimized at the cost of increase in logic gates and flip flops which generate the gated clock signal.

2. CLOCK GATING

In sequential circuit clock net is responsible for the power dissipation. Clock gating is the technique whose goal is to suppress the redundant transitions of the clock signal. The motivation of using clock gating is to shut down those block which are not doing any computation. Global clock is not provided to all the blocks in the circuit. It is given with an enable input signal.

PRINCIPLE OF CLOCK GATING:

When there is no change in the data input then global clock can be switched off till the time there is no transition on the data input[4]. Change in the input will generate clock gated signal with the help of enable signal. By doing this power of the clock can be saved.

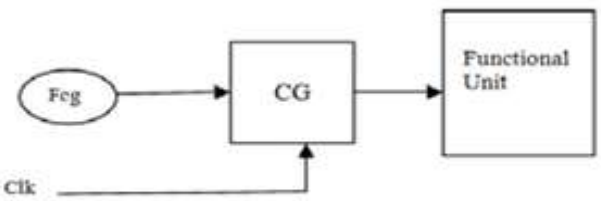

Fig. 1: Technique of Clock Gating

Many different technique[1] are available for clock gating: latch free clock gating (using AND and NOR gate), latch based clock gating, flip flop based clock gating, intelligent clock gating[1], IP level clock gating based design. Clock Gating is necessary because clock is fed to all the blocks in the sequential circuit and clock switches during every cycle. Clock system, composed by flip flop and clock distribution network is the most power consuming system. Clock gating reduces the power dissipation by selectively stopping the clock signal to that portion of the circuit which are inactive at that time. This paper implement the latch free clock gating design for D flip flop and LFSR and IP level adaptive clock gating for the UART on virtex6 FPGA. The power analysis [2] is represented in this paper of the circuits mentioned above with and without clock gating.

3. IMPLEMENTATION

The work of power optimization has been carried out by applying clock gating technique on D flip flop, Linear Feedback Shift Register, UART(Universal Asynchronous Receiver Transmitter) and analyze the circuit Power with or without clock gating.

A. D flip flop with clock gating

Latch free based design [3] clock gating technique [1] applied on the D flip flop. It is the simplest clock gating technique and make uses of AND and NOR gate for gating the clock signal. Monitoring the input and output of the flop via XOR gate will generate the enable signal for gating the clock signal.[3] When this enable signal will be high only then clock will be allowed to propagate to the flop.

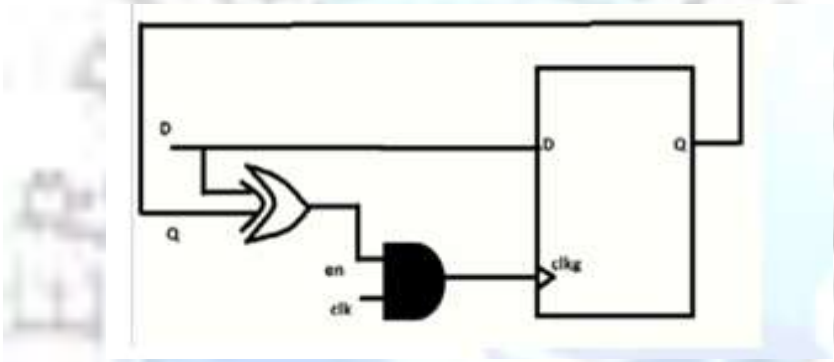

Fig. 2: Negative Edge DFF (Latch Free Based Design)

This AND gate just on and off the clock signal. For the correct operation the circuit imposes requirement that enable signal be held constant from active edge of the clock to inactive edge of clock to avoid the glitches in the clock.

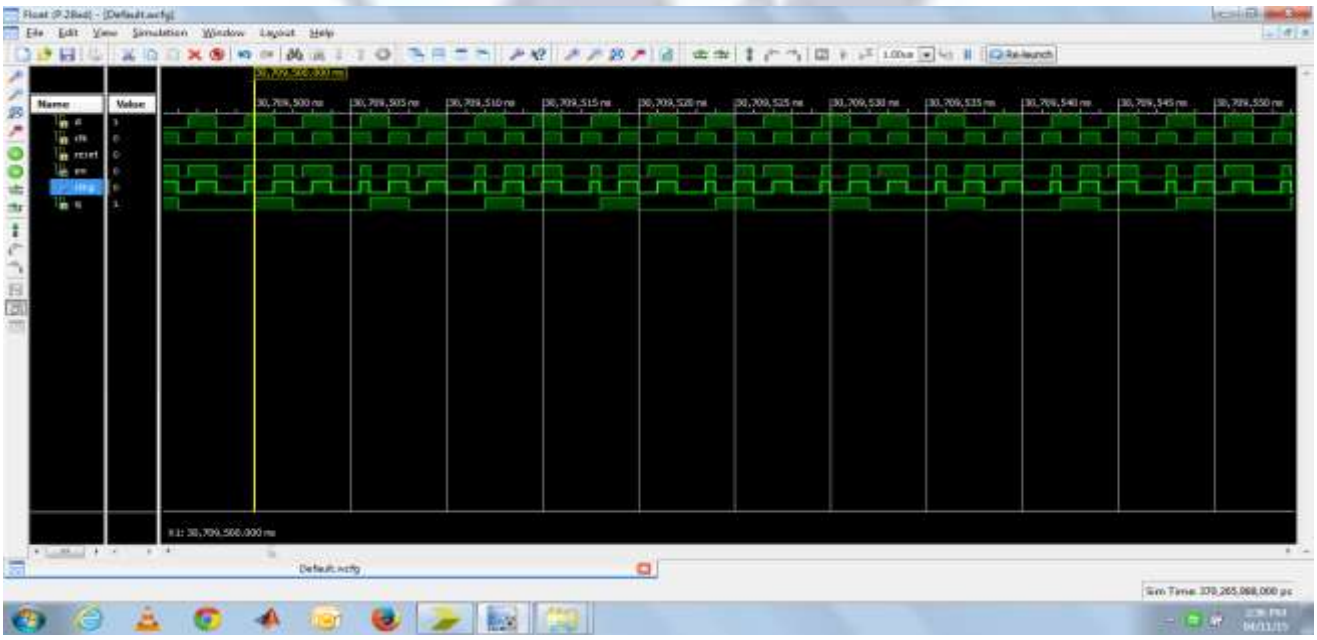

Fig. 3: Clock Gated D Flip Flop Waveform (Latch Free Based Design)

B. LINEAR FEEDBACK SHIFT REGISTER WITH CLOCK GATING

LFSR is a shift register [8] whose input is a linear function of its previous state. The linear function is exclusive-or (EX-OR) which is performed on the bits. An LFSR is a register whose input bit is driven by the XOR of some bits of some bits of the overall shift register value.

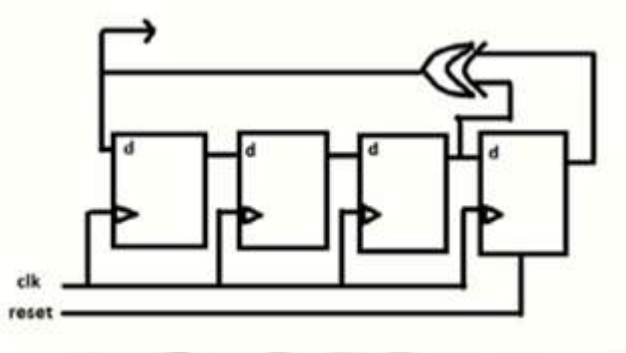

Fig. 4: Negative edge 4 bit LFSR

Initial value of the LFSR is called SEED. It comprises of 4 flip flops so there will be 4 enable signals generated for each case. Each flops input and output will be compared using XOR gate and then applied to the AND gate and this way generate the gated clock signal propagates to individual flop. Latch free based design clock gating applied to the circuit and circuit is simulated using ISIM simulator. Simulated waveform is shown in the figure:

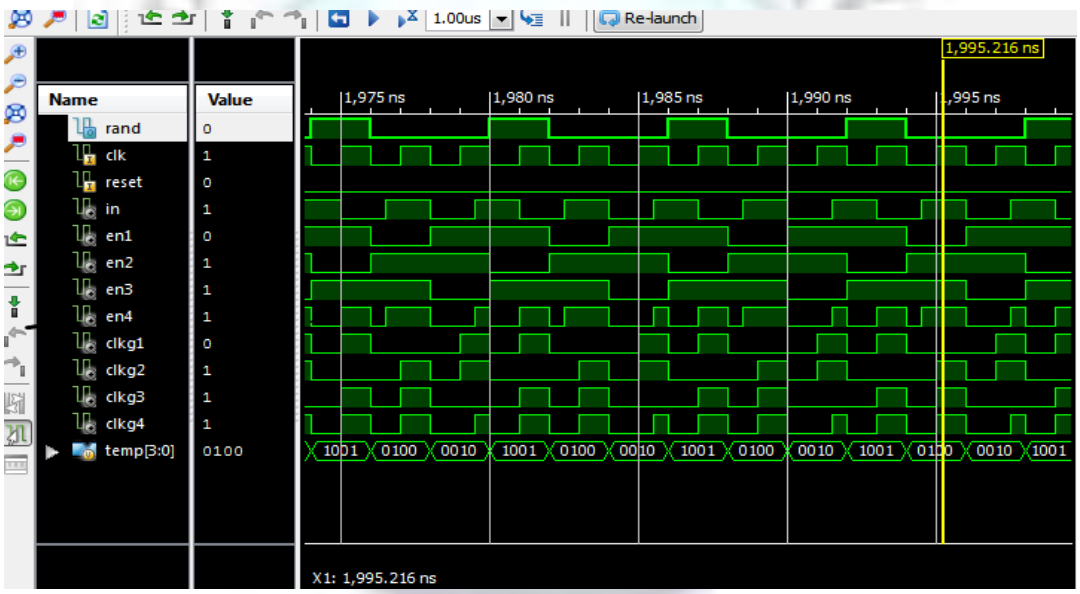

Fig. 5: 4 Bit LFSR Waveform (Latch Free Based Design)

C. UART (UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER):

UART is a piece of hardware that translates the data between serial and parallel forms. UART takes bytes of data and transmits the individual bits in a sequential fashion. At the destination, a second UART re-assembles the bits into complete bytes.

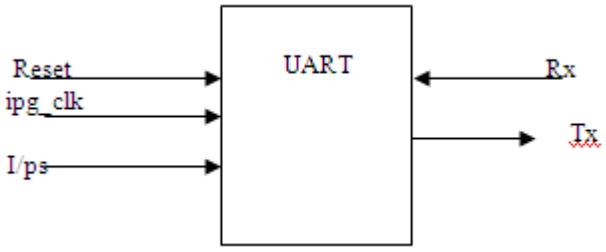

Fig. 6: UART

In UART there are two modules; one is transmitter module and other is receiver module. This can be modeled by Finite State Machine (FSM) which includes several states. Idle, Ready, Run and others. When an IP core finishes its work then it enters the IDLE state (IS) and stays there until it accept another request from the system bus to come in the working state. When UART works in the IDLE state it does not need the clock. Hence to disable the clock in this state clock gating can be used. If there is no new data pending to be transmitted the transmitters FSM will be kept shut off, the moment the clock gating hardware which is incorporated in the code sense arrival of any fresh data it starts supplying the clock signal. ADAPTIVE clock gating applied to UART in which clock gated enable signal is generated by user software.

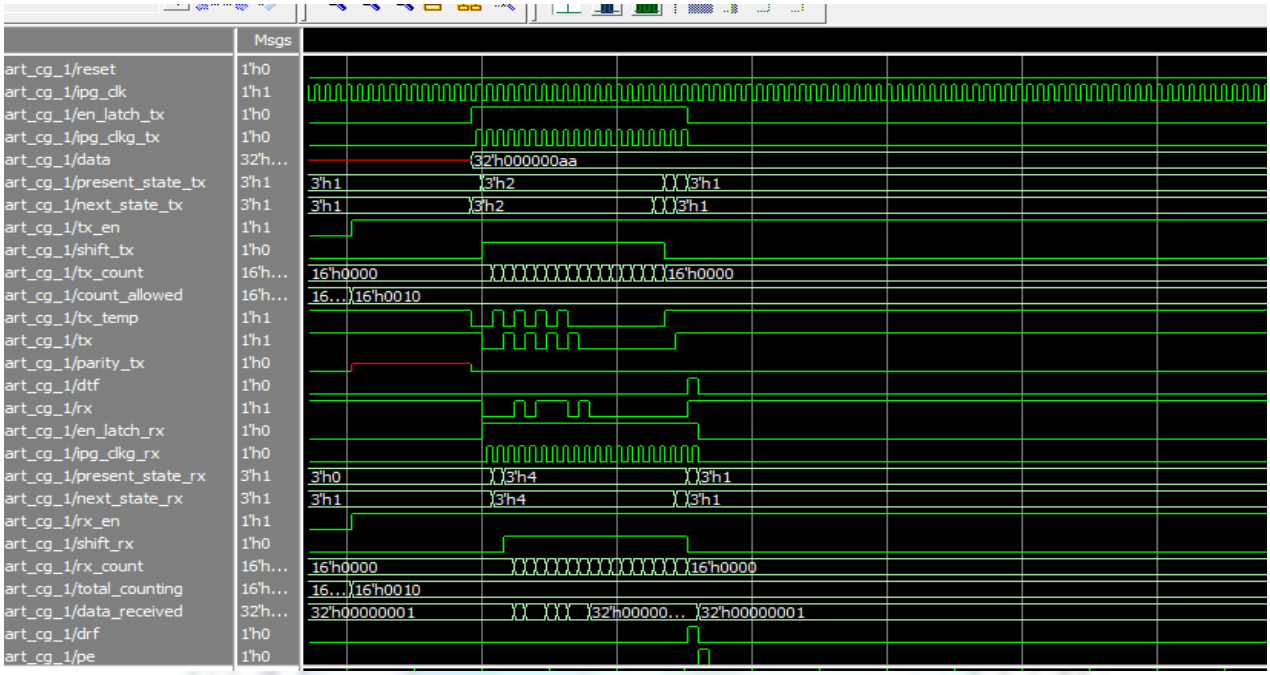

Fig. 7: Simulated waveform of UART

4. POWER ANALYSIS

Power of the circuits is calculated with or without clock gating. Power analysis is done using XILINX XPower Analyzer [2].

Table 1: Power of D Flips Flop without Clock Gating

Frequency	Dynamic	Total
10MHZ	0.00	1.293
100MHZ	0.004	1.296
500MHZ	0.018	1.311
1GHZ	0.036	1.329
10GHZ	0.367	1.668
100GHZ	3.670	5.049

Table 2: Power of LFSR without Clock Gating

Frequency	Dynamic	Total
10MHZ	0.00	0.162
100MHZ	0.006	0.165
500MHZ	0.015	0.176
1GHZ	0.021	0.180
10GHZ	0.145	0.303
100GHZ	1.373	1.538

Table 3: Power of UART without Clock Gating

Frequency	Dynamic	Total
10MHZ	0.001	1.294
100MHZ	0.09	1.131
500MHZ	0.045	1.132
1GHZ	0.090	1.212
10GHZ	0.895	2.017
100GHZ	8.769	9.891

From the results it is observed that clock power and the dynamic power increases with increase in frequency. At lower frequencies these variations are very less but as the frequency increases the variation also increases.

Table 4: Power of D Flip Flop with Clock Gating

FREQUENCY	DYNAMIC	TOTAL
10MHZ	0.00	1.293
100MHZ	0.00	1.293
500MHZ	0.001	1.294
1GHZ	0.002	1.295
10GHZ	0.036	1.329
100GHZ	0.357	1.658

Table 5: Power of LFSR with Clock Gating

Frequency	Dynamic	Total
10 MHZ	0.000	0.160
100MHZ	0.004	0.162
500MHZ	0.009	0.150
1GHZ	0.018	0.177
10GHZ	0.120	0.280
100GHZ	1.09	1.278

Table 6: Power of UART with Clock Gating

FREQUENCY	DYNAMIC	TOTAL
10MHZ	0.01	1.105
100MHZ	0.008	1.301
500MHZ	0.038	1.332
1GHZ	0.077	1.371
10GHZ	0.752	2.061
100GHZ	7.407	8.889

On implementing the clock gating on D flip flop and UART it is seen that there is reduction in the clock and dynamic power for lower frequencies. If the frequencies are higher then, temperature is beyond the limits and will give a very high power which is erroneous. The signal and IO power increases with clock gating due to additional hardware required to implement clock gating

CONCLUSION AND FUTURE ENHANCEMENTS

In this paper, clock gating technique is applied to a D flip flop, 4bit LFSR and UART and implemented on a 40nm virtex6 FPGA to reduce the clock power. The clock power is reduced by some extent at different frequency but extra hardware required for applying clock gating on the circuits. Area utilized for the clock gating is more but can be compensated for the reduction in power. Power reduction motivates this technique of clock gating. The future scope of this technology is that it can be implemented on other vertex series FPGA and also on the other application specific devices.

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