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Performance Analysis of Full Adder and Its Impact on Multiplier Design

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Abstract: **Full adder is an indispensable component for the design and development of all types of processors viz. digital signal processors (DSP), microprocessors etc. Adders are the core element of complex arithmetic operations like addition, multiplication, division, exponentiation etc. The various full adders available are conventional CMOS full adder, parallel prefix adders, hybrid full adders, mirror full adders, adders using mux and transmission gate logic. The main objective is to compare the existing full adder circuit's performance and to design a Low Power Full Adder and to analyze its impact on 4x4 Wallace Tree Multiplier design. The design and implementation of proposed full adder and multiplier is done by using Mentor Graphics tool in 180 nm technology.**

Index Terms: Delay, Full adder; Low Power; Performance Analysis; Logic Impact; Wallace Tree multiplier.

I. INTRODUCTION

The full adder is a basic building block of all digital VLSI circuits and has been undergoing a considerable improvement makes us to come out of our illusion that everything was done to the full adder. The secret behind this improvement is that the designers always targets on three basic design goals such as minimizing the transistor count, minimizing the power consumption and increasing the speed. In most of the cases, the full adder inevitably forms part of the critical path. So as a whole the full adder performance affects the system performance. A wide variety of full adders from the conventional to the hybrid and in different logic styles have been reported in the literature [1]-[11].

With the same motivation, our work involves the study of various popular adder structures and explores the performance parameters such as power dissipation and delay at different power supply voltages. The adders that are considered for this work include the conventional CMOS full adder [1], 16T full adder [2], 14T FA [3], 10T FA[4], 8T FA[5], mirror adder [6], multiplexer based adder [7], transmission gate based adder [8], conventional D3L[9], sp-D3L all three versions as in [10], BBL-PT Full adder[11]. A Wallace Tree Multiplier was designed with the above full adders.

II. Full Adder: Background

The updated literature survey reveals very wide spectrum availability of adder designs over the past few decades. Many designs of low power and high speed adder cells can be found in the literature. The conventional full adder performance is discussed in [11]. The contemporary designs include transmission gate (TGFA) [8], mirror FA [11], mux based FA [7], and spi-D3L [12] are explored. The full adder cell realization of the circuit using 16 T, 14T, 10T and 8T are available in [5].

III. PERFORMANCE ANALYSIS AND COMPARISON

The performance of a full adder circuit depends greatly on the type of design used for implementation and also on the logic function realized using the particular design style. A conventional CMOS design allows circuits to have a reasonable power delay product (PDP) but dynamic design styles gives fast design with high power consumption. Hence, an analysis and its impact on other logic functions is very much in demand.

All the adder circuits described in [1]-[12] were implemented in 180-nm CMOS process.

A. Power Dissipation Comparison

Table I shows the performance comparison of the adder circuits operated at 1V, 1.5V, 2V, 2.5V supply voltage and

1GHz measurement frequency. The table indicates the average power consumption when executing the set of all possible input combinations to the adders.

B. Delay comparison

Table II presents the delay comparison of all the full adder circuits operated at 1V, 1.5V, 2V, 2.5V supply voltage and 1GHz measurement frequency. The delays reported correspond to the worst case delays observed in every adder.

C. Power Delay Product

Table III shows the power delay product of all the full adder circuits operated at 1V, 1.5V, 2V, 2.5V supply voltage and 1GHZ measurement frequency. The power delay product reported is multiplication of the average power consumption when executing the set of all possible input combinations to the adders and worst case delays observed in every adder

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Table I: Power Dissipation (NW) Of Full Adders at Different Supply Voltages

Voltage	28T	16T	14T	10T	8T	Mirror	TGFA	Spi1	Spi2	Spi3	ConD3L	Mux	BBLPT
1V	15.82	13.2	11.60	10.0	8.3	15.82	16.97	37.88	38.03	46.88	19.84	13.56	26.17
1.5V	31.76	27.81	43.98	22.49	18.00	31.76	28.36	78.48	78.44	97.42	40.68	23.83	54.75
2V	56.21	50.92	106.7	39.99	28.61	56.21	48.23	142.39	141.99	177.12	73.20	31.99	100.10
2.5V	91.66	85.04	207.4	62.49	32.51	91.66	51.82	236.46	235.39	294.53	120.77	49.99	167.05

Table II: Delay (NS) Of Full Adders At Different Supply Voltages

Voltage	28T	16T	14T	10T	8T	Mirror	TGFA	spi1	Spi2	Spi3	ConD3L	Mux	BBLPT
1V	19.84	19.61	19.53	19.49	19.3	20.01	49.99	20.89	20.89	19.46	29.91	29.7	49.98
1.5V	19.88	19.73	19.66	24.23	19.4	22.16	49.99	25.06	24.22	22.16	31.38	31.7	49.85
2V	24.07	19.83	19.85	26.34	19.6	23.72	49.99	33.64	25.01	23.72	34.78	34.8	49.70
2.5V	35.35	19.85	21.53	28.31	19.7	29.99	49.99	39.33	29.99	29.99	39.93	38.0	49.52

Table III: Power Delay Product (PDP W-S) Of Full Adders at Different Supply Voltages

Voltage	28T	16T	14T	10T	8T	Mirror	TGFA	spi1	Spi2	Spi3	ConD3L	Mux	BBLPT
1V	313.9	258.8	226.5	194.2	160	316.02	848.33	791.31	794.8	912.28	593.41	402	1308
1.5V	631.3	548.6	864.2	544.9	349	703.80	1417.6	1967.2	1899.8	2158.3	1276.6	755	2729
2V	1352.	1009.	2117.	1053	560	1333.3	2411.0	4790.3	3551.4	4201.2	2545.0	1113	4976
2.5V	3240.	1688.	4465.	1769	640	2748.8	2590.4	9300.2	7059.3	8832.9	4822.5	1899	8273

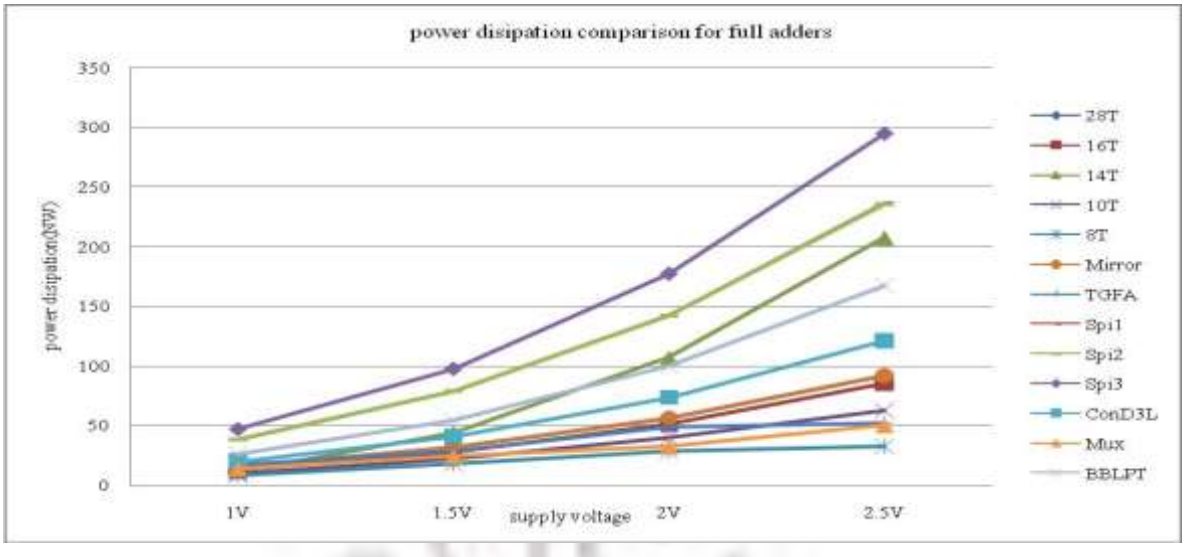

Fig: 1: Analysis of Power Dissipation for Different Full Adders

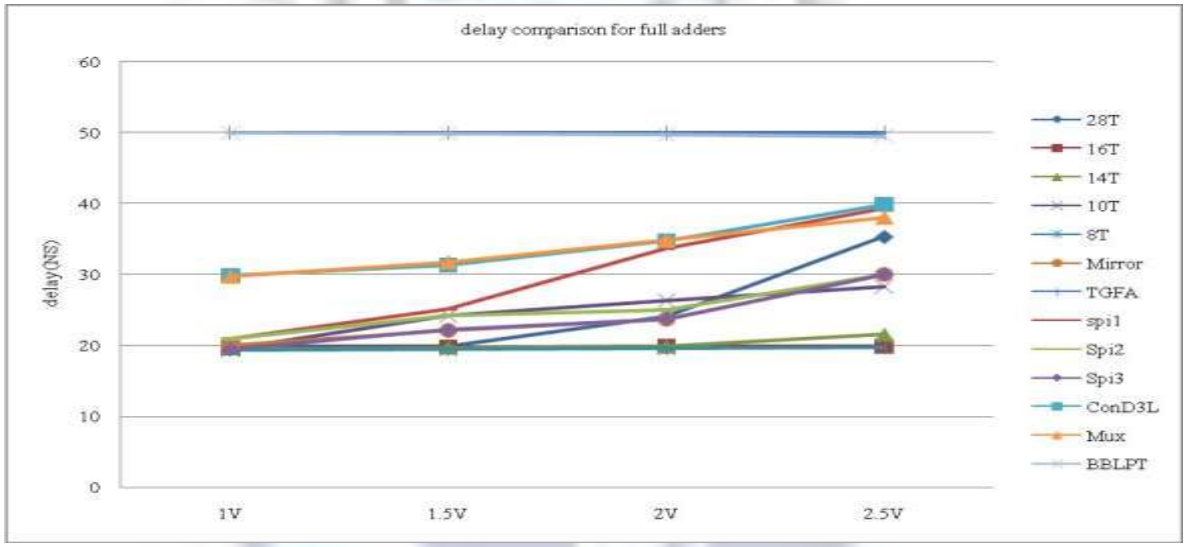

Fig: 2: Delay Comparison For Full Adder

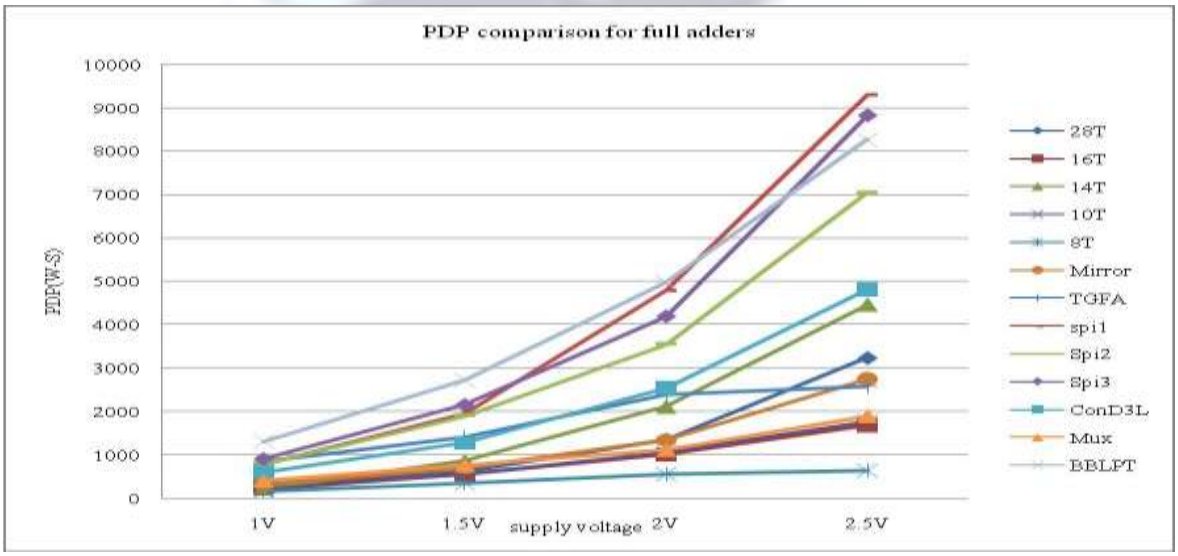

Fig: 3: PDP Comparisons for Full Adders

IV. IMPACT ON MULTIPLIER DESIGN

Moreover, we constructed an 4x4 Wallace tree multiplier to evaluate the performance of full adders in a realistic way. The Wallace tree multiplier topology employs an array of full adder cells in cascaded structure. The full adders are driving each other and hence explored the impact of full adders driving each other with different loading and timing characteristics. Table IV presents the performance of Wallace tree multiplier using different full adders. Table V reports the delay of Wallace tree multiplier using different full adders. The power delay product of the 4x4 multiplier using different full adders is shown in Table VI.

Table IV: Power Dissipation (W) Of Wallace Tree Multiplier at Different Supply Voltage.

Voltage	28T	16T	14T	10T	8T	Mirror	TGFA	Spi1	Spi2	Spi3	ConvD3L	Mux	BBLPT
1.5V	2.14	2.14	2.14	2.14	2.14	2.14	2.14	2.10	2.14	2.14	2.14	2.14	2.144
2V	4.86	4.86	4.86	4.88	4.86	4.86	4.86	4.85	4.86	4.86	4.86	4.86	4.86
2.5V	8.58	8.58	8.58	8.99	8.56	8.58	8.58	8.58	8.58	8.58	8.58	8.58	8.58

Table V: Delay (NS) Of Wallace Tree Multiplier at Different Supply Voltages

Voltage	28T	16T	14T	10T	8T	Mirror	TGFA	spi1	Spi2	Spi3	ConD3L	Mux	BBLPT
1V	28.74	24.91	41.96	23.58	9.59	29.54	50.0	50.08	50.06	13.86	29.29	34.92	35.91
1.5V	44.15	25.07	42.40	24.59	9.89	44.15	50.04	50.09	49.89	24.06	29.41	35.51	36.87
2V	45.92	37.78	44.83	37.68	27.3	46.39	50.04	49.81	29.42	26.86	49.57	37.55	38.09
2.5V	46.88	41.58	48.18	37.95	37.5	48.43	59.99	49.78	49.75	31.45	49.91	37.96	42.66

Table VI: Power Delay Product (PDP N-S) Of Wallace Tree Multiplier at Different Supply Voltages

Voltage	28T	16T	14T	10T	8T	Mirror	TGFA	spi1	Spi2	Spi3	ConD3L	Mux	BBLPT
1.5V	94.68	53.77	90.9	52.62	21.20	94.68	107.2	105.6	106.7	51.48	62.93	76.1	79.06
2V	223.3	183.6	217.	184.2	132.7	225.5	243.3	241.8	142.9	130.5	240.91	182.	185.2
2.5V	402.3	356.8	413.	341.4	321	415.7	514.9	427.1	426.8	269.8	428.22	325.	366.1

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TABLE VII: PDP (w-s) Comparison of Multiplier for Supply Voltage 1v

TYPE OF FULL ADDERS	PDP(W-S)
28T	12297.9
16T	10662.2
14T	17953.4
10T	4253.44
8T	4103.21
Mirror	12643.02
TGFA	21404.6
Spi1	21443.7
Spi2	21438.06
Spi3	21380.6
ConvD3L	10092.4
Mux	14944.8
BBL-PT	5933.59

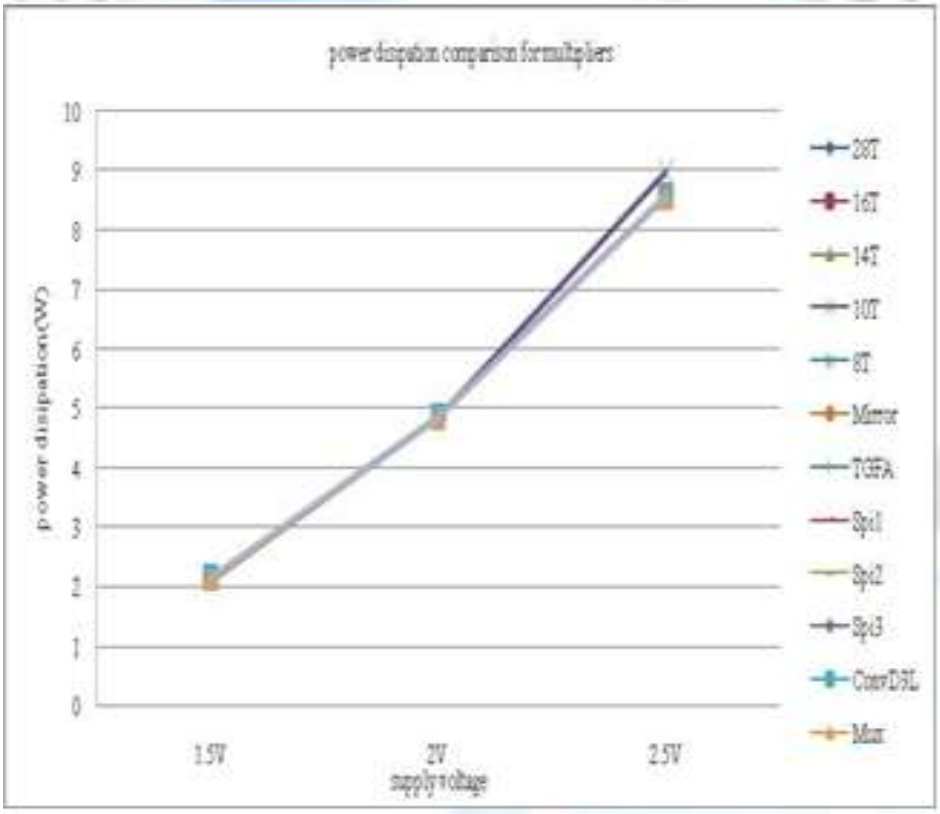

Fig: 4: Power Dissipation Comparison For Multipliers

Table VIII: Power Dissipation (Mw) Of Multiplier For Supply Voltage 1v

TYPE OF FULL ADDERS	POWER DISIPATION
S28T	427.888
16T	427.872
14T	427.87
10T	427.864
8T	427.134
Mirror	427.888
TGFA	427.871
Spi1	428.156
Spi2	428.196
Spi3	428.307
ConvD3L	427.927
Mux	427.864
BBL-PT	427.893

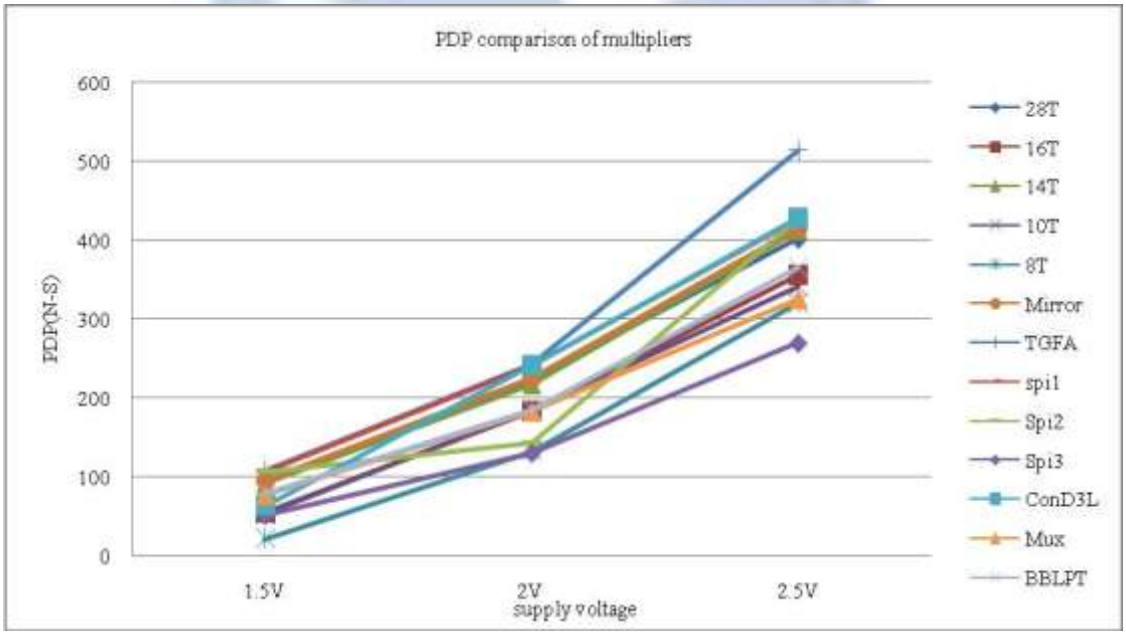

Fig: 5: Delay Comparison For Multipliers

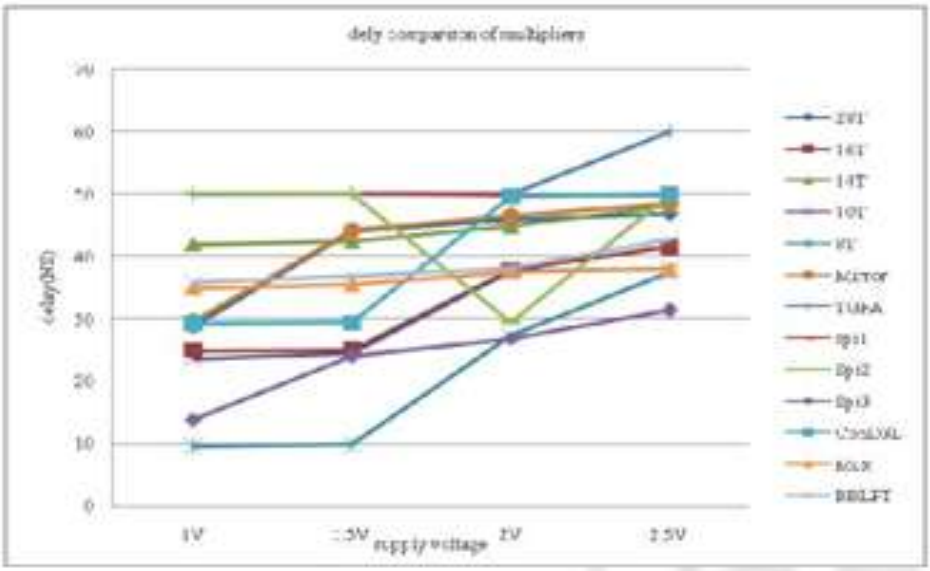

Fig: 6: PDP Comparison For Multipliers

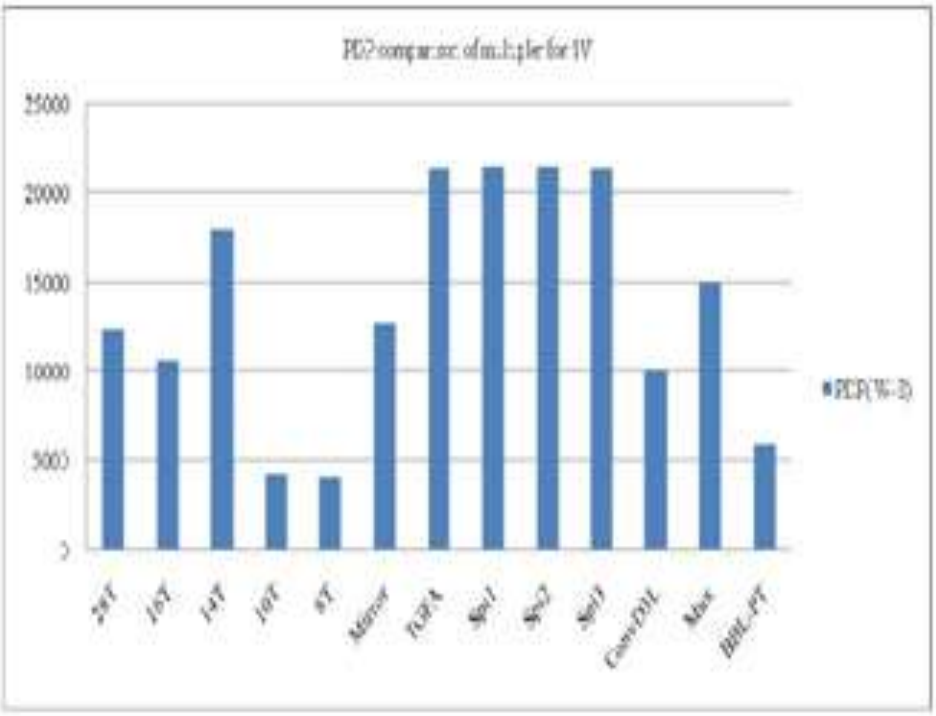

Fig: 7: PDP Comparison of Multiplier for Supply Voltage 1v

CONCLUSION

Based on the performance analysis, it is observed that the 8T FA is superior in terms of low power dissipation and high speed. At the same time for the same operating conditions, 10T FA is low power dissipation with more delay. Spi3 provides less delay but suffers with high power dissipation. The required adder can be chosen from the performance analysis tables to meet the design specifications such as low power dissipation, less delay.

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