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# A New design of 1-bit full adder based on XOR-XNOR gate

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**Abstract: In this paper propose a new high performance 1 bit full adder cell using XOR/XNOR gate design style as well as lower power consumption. Simulation results illustrate the superiority of the resulting proposed adder against conventional 1-bit full-adder in terms of power consumption improvement performance (98% of 10T, 47% of 14T & 16T), propagation delay and PDP. We have performed simulations using TSPICE in a 0.180µm standard CMOS technology.**

**Keywords: XOR-XNOR Gate, Delay, Power Delay, full adder**

## I. INTRODUCTION

Low power and High speed are the design trade-offs in VLSI industry. Ever since its inception, the design of full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing a considerable improvement, being motivated by three basic design goals, viz. minimizing the transistor count, minimizing the power consumption and increasing the speed, [4].Most of the VLSI applications, such as digital-signal processing and microprocessors, use arithmetic operation. Addition, subtraction, multiplication, and multiply and accumulate (MAC),[5] are examples of the most commonly used operations .The growth of portable devices like PDAs, cell phones, etc, demand high speed processing capabilities that also consume less power. The1-bit full adder is the building block of these operation modules. Thus, enhancing its performance is critical for enhancing the overall module performance. In this paper, we present a novel 1-bit full-adder cell using XOR-XNOR circuit [8], which offers faster operation, and consumes less power than the other proposed full-adder cell based on XOR-XNOR gates.

The rest of the paper is organized as follows: In section II,we present the mathematical equations which lead to construction of new full adders. In section III, some standard implementations of the full adder cell is discussed asprevous work. In section IV, shows The new proposed full adder cells are described in section V. Simulation results for proposed and existing designs are given and comparisons are carried out. In section VI wave form of proposed full adder s shown.

## II. MATHEMATICAL EQUATIONS FOR FULL ADDERS

We now present the mathematical equations which lead to the design of the new full adder cells. The addition of two bits A and B with Cin yields a SUM and a Cout bit. The general equations for SUM and Cout are given below:

$$\mathrm{SUM} = \mathrm{A} \oplus \mathrm{B} \oplus \mathrm{Cin} \quad (1)$$

$$\mathrm{Cout} = (\mathrm{A} \oplus \mathrm{B})\mathrm{Cin} + \mathrm{AB} \quad (2)$$

These two equations can be rearranged as follows:

$$\mathrm{SUM} = (\mathrm{A} \oplus \mathrm{B})\mathrm{Cin}' + (\mathrm{A} \odot \mathrm{B})\mathrm{Cin} \quad (3)$$

$$\mathrm{Cout} = (\mathrm{A} \odot \mathrm{B})\mathrm{Cin}' + (\mathrm{A} \oplus \mathrm{B})\mathrm{Cin} \quad (4)$$

## III. PREVIOUS WORK

**M. Vesterbackaet al. [2],** the 16 transistor full adder circuits is designed using 6T XOR-XNOR circuit, one CMOS inverter and a multiplexer as shown in Figure.1. So, the circuit has a low device count, and also has full voltage-swing. Author also proposed another full adder circuit having 14 transistors as shown in Figure2 .The circuit is composed of cross coupled pMOS FET and complementary cross coupled nMOSFET. These structures do not provide an output for A = B = 0 and A = B = 1, respectively, which is provided by the feedback of nMOSFET and pMOSFET marked with asterisks (*) in figure 2.

**D. Wang, M. Yanget al.[3],** the 1 bit full adder circuit is designed using 3T XOR ,3T XNOR gate and two multiplexer as shown in Figure.3,the C input signal, which has full voltage swing and no extra delay, is used to drive the multiplexers, thereby reducing the overall delay.

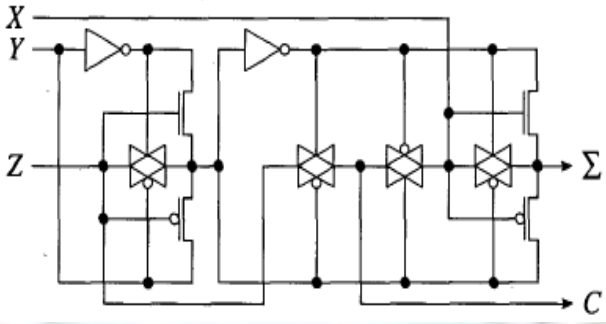


**Figure. 1: 16-Transistor full adder circuit [2]**

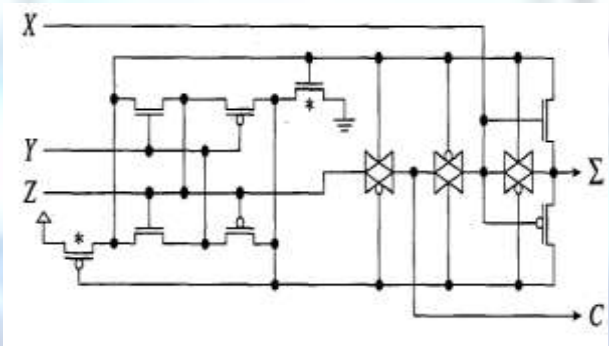


**Figure. 2: 14-Transistor full adder circuit [2]**

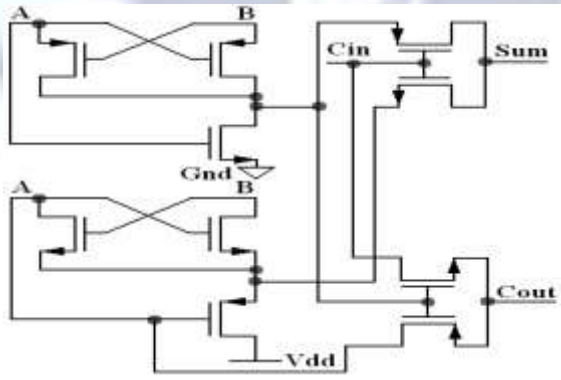


**Figure. 3: 10-Transistor full adder circuit [3]**

## IV. PROPOSED 9-TRANSISITOR FULL ADDER

The proposed full adder consists of two modules, including one 5-T XOR-XNOR gate, and two 2-T multiplexers (2-T MUX).As shown in the equations (3) and (4) above, XOR and XNOR gates are the essential parts in full adders. The authors provide a 5T XOR-XNOR gates to improve the performance of full adders [1]. The XOR-XNOR gate described in [1] is shown in Figure 4. However, these XOR and XNOR gates give bad output logic levels for certain input combinations. This problem can be solved by manipulating the (W/L) ratios of PMOS and NMOS transistors, which restores the logic levels to an acceptable level.

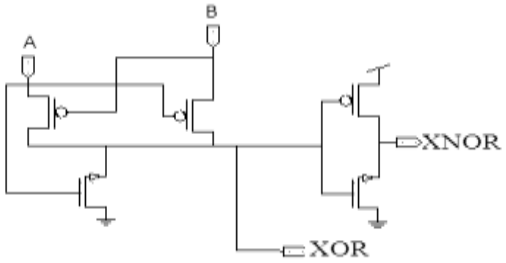


**Figure. 4: 5-Transistor XOR-XNOR gate**

The proposed full adder circuit is shown below in figure 5.
The operation of the proposed circuit can be understood by Table 1.

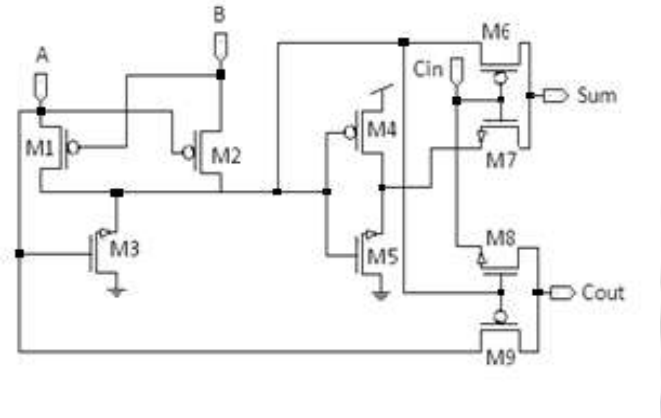


**Figure. 5: Proposed 9-transistor full adder circuit**

## V. Simulation Results of 9- Transistor full adder circuit

The full adder circuit is simulated using HSPICE at voltage 5V using 0.180µm CMOS technology .The delay has been measure between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of voltage level for both rising and fall transition for Sum and Cout. The power delay product (PDP) is measured as the product of the average delay and the average power. The output waveform of the proposed circuit is shown in figure 6.
The comparison of delay for Sum and Cout, and average power consumption of the proposed circuit with different circuits discussed in literature is shown in Table 2. XOR-XNOR circuits for each input combination are shown in Table 2. The results of simulation which included a delay and power dissipation are listed in Table 2 are also represented in Figure (7) and (8). The results indicate that the delay of the proposed full adder circuit is smaller than previous circuit in Figure 1[5], 2[2] and 3[4]. Regarding to the simulation results, the proposed XOR-XNOR circuit are the most energy efficient and very well suited to low voltage applications.

**WAVE FORM OF PROPOSED FULL ADDER**

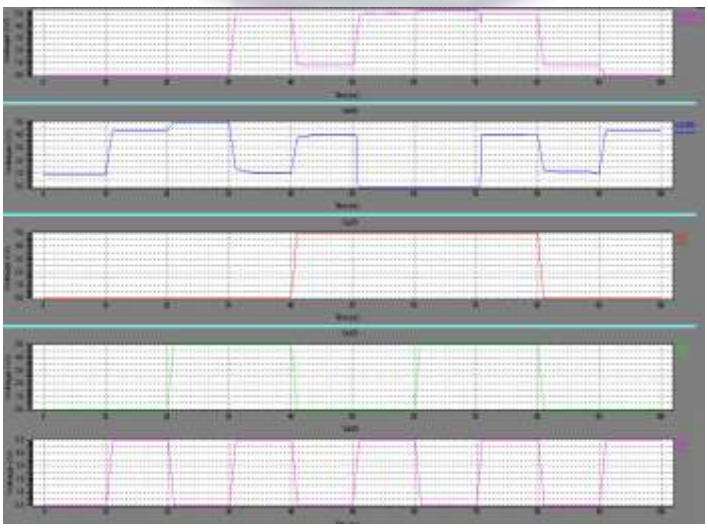

**Figure. 6: Output Waveform of proposed adder**

**Table: 1. Truth table for SUM Full adder**

| Full Adder | Rising delay (*) | Falling Delay (*) | Propagation delay( )* | Power consumption($) | PDP (&) |
|---|---|---|---|---|---|
| 9T(prop) | 19.8 | 20 | 19.9 | .082 | 1.63 |
| 10T | 20 | 20 | 20 | 5.6 | 112 |
| 14T | 29.6 | 29.7 | 29.6 | .155 | 4.5 |
| 16T | .004 | .005 | .004 | .155 | .0006 |
| Units- *=ns,$=pw, &=ns x ns | | | | | |

**Table: 2. Truth table for Carry Full adder**

| Full Adder | Rising delay (*) | Falling Delay (*) | Propagation delay( )* | Power consumption($) | PDP (&) |
|---|---|---|---|---|---|
| 9T | 20 | 40 | 30 | .082 | 2.46 |
| 10T | 20 | 50 | 35 | 5.6 | 196 |
| 14T | .009 | .003 | .006 | .155 | .0009 |
| 16T | 20 | 40 | 30 | .155 | 4.65 |
| Units- *=ns,$=pw, &=ns x ns | | | | | |

## VII. COMPARISON OF DELAY FOR SUM AND CARRY

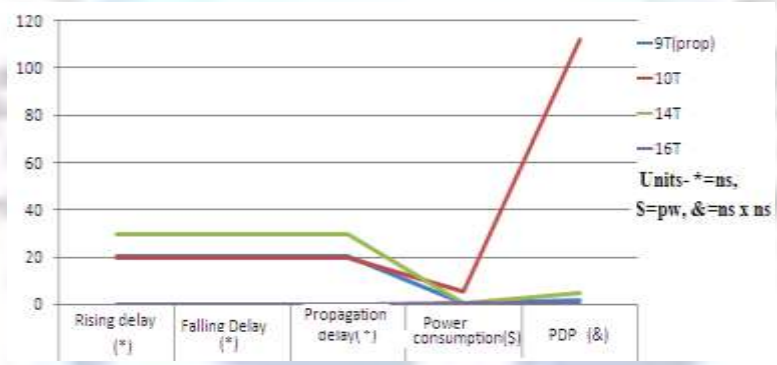


**Figure.7: Comparison of delay for Sum**

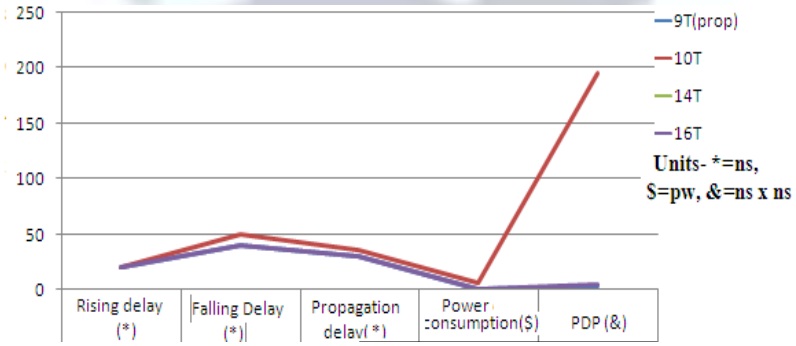


**Figure. 8: Comparison of delay for Cout**

## CONCLUSION

A novel 1-bit full adder cells using the existing XOR/XNOR gates have been proposed. The power dissipation, propagation delay and power-delay product of the proposed adders have been compared with the existing adders and are found to be efficient. Simulations show that the proposed full-adders outperform its counterparts exhibiting an power consumption improvement performance (98% of 10T, 47% of 14T & 16T), propagation delay and PDP.

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| INPUT | | | ON/OFF TRANSISTOR | | | | | | | | | OUTPUT | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | M1 | M2 | M3 | M4 | M5 | M6 | M7 | M8 | M9 | SUM | Cout |
| 0 | 0 | 0 | ON | ON | OFF | ON | OFF | ON | OFF | OFF | ON | 0 | 0 |
| 0 | 0 | 1 | ON | ON | OFF | ON | OFF | OFF | ON | OFF | ON | 1 | 0 |
| 0 | 1 | 0 | OFF | ON | OFF | OFF | ON | ON | OFF | ON | OFF | 1 | 0 |
| 0 | 1 | 1 | OFF | ON | OFF | OFF | ON | OFF | ON | ON | OFF | 0 | 1 |
| 1 | 0 | 0 | ON | OFF | ON | OFF | ON | ON | OFF | ON | OFF | 1 | 0 |
| 1 | 0 | 1 | ON | OFF | ON | OFF | ON | OFF | 0N | ON | OFF | 0 | 1 |
| 1 | 1 | 0 | OFF | OFF | ON | ON | OFF | ON | OFF | OFF | ON | 0 | 1 |
| 1 | 1 | 1 | OFF | OFF | ON | ON | OFF | OFF | ON | OFF | ON | 1 | 1 |