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# FPGA Implementation of 2D Discrete Wavelet Transform in Video Signal Processing

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**Abstract: In the world of social media video processing is very popular. A video signal is the term used to describe any sequence of time varying images. This paper presents the architectures for Video Processing algorithm using softcore processor. This hardware/software co-design platform has been implemented on a Xilinx Virtex-5 FPGA (XUPV5-LX110T). Field Programmable Gate Array (FPGA) offers various resources which can be programmed for building up an efficient embedded system. The system consists of Microblaze and some IP core provided by Xilinx. Soft-core processors are complete microprocessors described in a hardware description language (HDL) such as VHDL, Verilog, etc. Advantages of Softcore Processors are more flexible, Platform independent, high level of abstraction, etc. The aim of this paper is to perform video compressing using discrete wavelet transform (DWT). The DWT was based on time-scale representation, which provides efficient multi-resolution. Video processing applications including video encoding/decoding, surveillance, detection and recognition.**

**Keywords: DWT/IDWT, FPGA, Microblaze, Video Compression.**

## Introduction

The meaning of video is the motion pictures. Video is a term used to describe any sequence of time varying images. Movies or films, digital cameras and television are some examples of video signals as are the signals that drive computer monitor, laptop, mobile and PDA displays. Video is made up of number of frames that are projected at proper rate 30 fps to desired. Though without noticing, a growing percentage of the world population uses presently image, video and audio compression technologies on a rather regular basis. The compression of an image or video file is of great concern in digital communication system because of the storing capacities and constraints in the transmission rate.

FPGA are the integrated circuits of which their hardware configuration can be changed by the user according to the desired functions. The most important features of FPGAs are the ability to do parallel processing, and opportunity to change the internal structure and its function according to the desired application. The meaning of parallel processing is the ability to make multiple transactions at the same time. Microblaze is soft processor consisting around 900 LUTs. For video processing using Soft core Processor, we will create a soft processor using Xilinx Platform Studio software. We will program the processor with C language and finally we will download the processor to FPGA on the development board.

The raw or uncompressed videos require large data to be stored or transmitted which is a major challenge for digital video signaling. The main purpose of image and video compression is to represent (or encode) a digital image or sequence of images (video) using very few bits for maintaining its visual appearance [4]. By minimizing the spatial and temporal redundancies present in the video signals, video compression can be easily achieved [3]. In signal processing there are several common transforms, such as Discrete Fourier Transform (DFT), Discrete Cosine Transform (DCT) & Discrete Wavelet Transform (DWT) etc. The most commonly used transform for processing images and videos is the DCT [8]. But, comparing to DCT, the DWT seems to have better performance for image and video coding. DWT also provides us the scalability functionalities of image and video [9].

## Discrete Wavelet Transform

The wavelet transform provides a time-frequency representation of the signal. Wavelet transform are localize in both time and frequency domain. The advantage of the Discrete Wavelet Transform over Fourier transformation is to performs multi-resolution analysis of signals with time-frequency localization. The multi-resolution is to represent a signal with a set of coefficients, each of which provides information about the position and the frequency of the signal. The 2D Discrete Wavelet Transform (DWT) is an important function in many multimedia applications, such as JPEG2000 and MPEG-4 standards, digital watermarking, and content-based multimedia information retrieval systems.

There are several steps discuss here to perform DWT are firstly replace each row with its 1-D DWT. Second step is Replace each column with its 1-D DWT. Third step is Repeat steps 1 & 2 on the lowest subband for the next scale. Forth step is repeat step 3 until as many scales as desired.

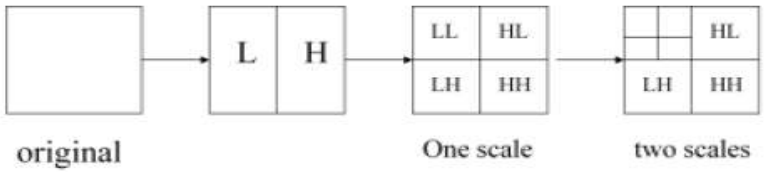


**Fig. 1 Steps for Wavelet Transform**

## FPGA Design

FPGA is basically consists of matrix of Logic Cells called as sclices, I/O Blocks (Input/ Output) and interconnections. Logic Cells form a main structure of FPGAs. A Logic-Cell consists of one Lookup Table (LUT), one D-Flip Flop and one 2 to 1 Multiplexer. LUTs are actually small memories (RAM) that fulfill logic operations. Interconnections of logic cells are provided by programmable switches and matrix formed data paths (according to the installed program FPGA).

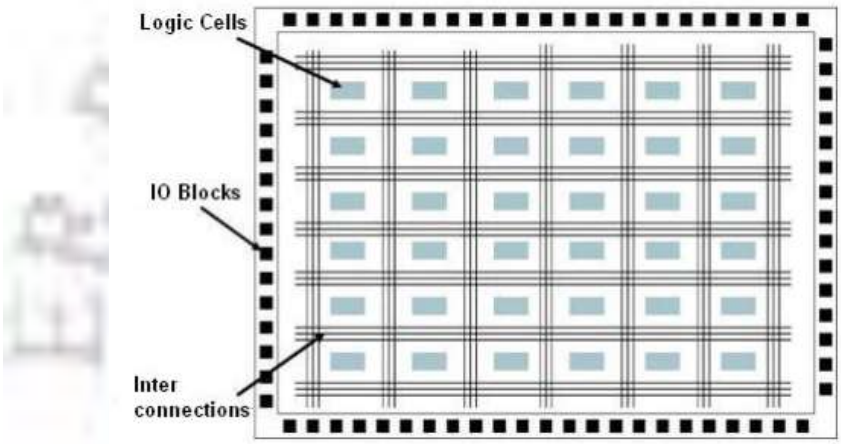


**Fig 2 FPGA Architecture**

The board used for Video Processing is the Virtex-5 ML505 Evaluation Platform developed by Xilinx. This board has a Xilinx Virtex-5 XC5VLX110T FPGA with 69,120 logic cells, 64 DSP48Es, and 5,328Kb of block ram (BRAMs). The board has an Analog to Digital Converter (ADC) AD9980 for video input. The XUPV5-LX110T MicroBlaze design hardware includes DDR2 Interface (256 MB), BRAM, External Memory Controller (EMC), Networking, UART, GPIO (IIC, LEDs and LCD) etc. Moreover, the board has a Digital to Analog Converter (DAC) CH7301C for video output. It is a display controller device which accepts a digital graphics input signal, and encodes and transmits data through DVI (Digital Visual Interface). On the Virtex-5, the definition of a CLB is two slices, and each slice contains four 6-input LUTs, four flip-flops, wide-function multiplexers, and carry logic. Some new terms SLICEL and SLICEM are defined on the Virtex-5, SLICEL are base slices. Some slices have built-in distributed RAM and 32-bit shift registers. Slices with these additions are called SLICEM.

TABLE I: Components of a CLB on the Virtex-5

| Slices | LUTs | Flip-Flops | Arithmetic and Carry Chains | Distributed RAM[1] | Shift Registers[1] |
|---|---|---|---|---|---|
| 2 | 8 | 8 | 2 | 256 bits | 128 bits |

[1]SLICEM only

## MICROBLAZE

The MicroBlaze embedded soft core is a reduced instruction set computer (RISC) optimized for implementation in Xilinx field programmable gate arrays (FPGAs). See Figure 3 for a block diagram depicting the MicroBlaze core. The MicroBlaze embedded soft core includes the features like Thirty-two 32-bit general purpose registers, 32-bit instruction

word with three operands and two addressing modes, Separate 32-bit instruction and data buses with direct connection to on-chip block RAM through a LMB (Local Memory Bus), 32-bit address bus, FSL (Fast Simplex Link) support, etc. Processor is created in Xilinx Platform Studio Software. The processor design is automatically created by using (BBW) Base System Builder Wizard in Xilinx Platform Studio. MicroBlaze is a virtual processor that is constructed by combining the blocks called cores in Xilinx FPGAs. Because It can be created more than one processor in a FPGA and it can also be added any number of core to the processor.

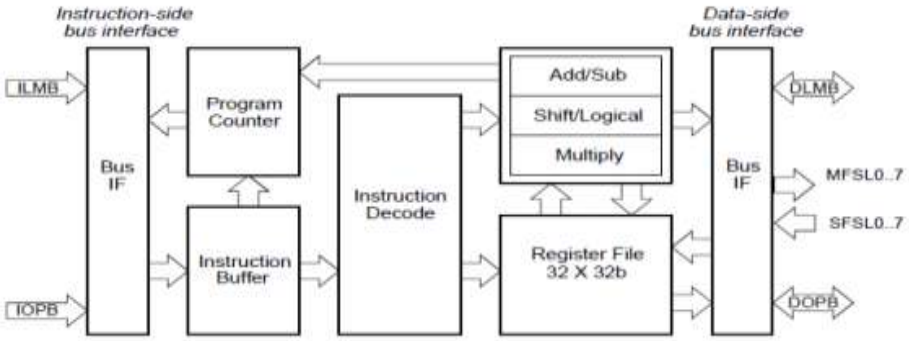


**Fig. 3: Block diagram of Microblaze architecture**

## PROPOSED ARCHITECTURE

Now a days, the main problem related to good clarity video is its large size, So that video compression is required to save storage space. Here we are presenting a DWT approach to perform the video compression. The most common compression techniques find the redundancies in the movie frame and the correlation between the scenes to get high degree of compression.

### Discrete Wavelet Transforms:

The DWT is popularly used for image and video compression because of the DWT supports features like progressive image transmission, region of interest coding, etc. The most important characteristic about the DWT is the DWT has new JPEG2000 image compression standard.

### A. One-Dimensional Discrete Wavelet Transform

Two main methods exist for the implementation of 1D-DWT: the traditional convolution-based implementation and the lifting-based implementation [1].

### B. Two-Dimensional Discrete Wavelet Transform

The basic idea of 2-D architecture is similar to 1-D architecture. There are several steps to perform 2D DWT. A 2D DWT can be seen as a 1-D wavelet scheme which transform along the rows and then a 1-D wavelet transform along the columns are shown in fig 1. Here, f[n] is the 1D input signal and f′ [n] is the reconstructed signal. h[−k] and g[−k] are the lowpass and highpass analysis filters, while the corresponding lowpass and highpass synthesis filters are h[k] and g[k]. $C_j$ and Dj are the low-band and high-band output coefficients at level j. DWT analysis, or decomposition, is, mathematically,

$$Cj\,[k] = (C_{j+1}[k] * h[-k]\,) \downarrow 2, \tag{1}$$

And

$$Dj\,[k] = (C_{j+1}[k] * g[-k]\,) \downarrow 2, \tag{2}$$

Where $*$ denotes convolution and $\downarrow 2$ denotes downsampling by a factor of two. That is, $y[n] = x[n] \downarrow 2$ then

$$y[n] = x[2n]. \tag{3}$$

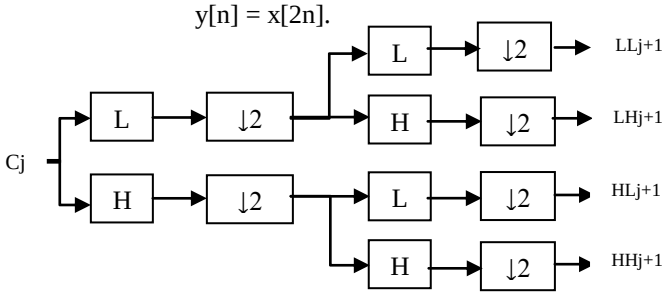


**Fig. 4 Wavelet decomposition**

The outputs of highpass and lowpass filters are called DWT coefficients and these coefficients can processed in reverse order to reconstruct the original image or signal which is called inverse discrete wavelet transform (IDWT) [10].

In inverse wavelet transformation, the coefficients in wavelet domain are converted into spatial domain. The corresponding operation of DWT synthesis, or reconstruction, is

$$C_{j+1}[k] = (C_j[k] \uparrow 2) * h[k] + (D_j[k] \uparrow 2) * g[k] \quad (4)$$

Where ↑2 denotes upsampling by a factor of two. That is if, y[n] = x[n] ↑2, then

$$y[n] = \begin{cases} x\left[\frac{n}{2}\right] \\ 0 \end{cases} \quad (5)$$

From the inverse transformation process, the decompressed video frames are finally obtained.

First we input the video generally .avi format video, then analyze video format those are AVI or not. Then extract all the frames from a video. Apply DWT compression to each frame and sort the frames numbers to analyze the result. Proposed model shows in figure 5.

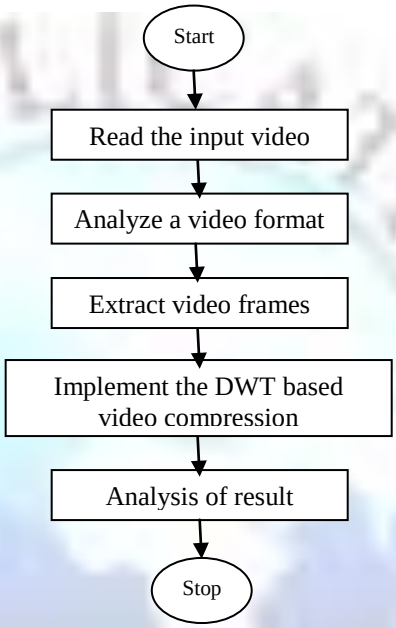


**Fig 5 design flow chart**

## RESULTS

The proposed algorithm is implemented using Xilinx ISE Design Suite 13.1. First create the Microblaze processor using Xilinx Platform Studio. Add peripherals which are require for video processing like SRAM, UART etc while creating a system. Then export design SDK and write embedded C code for video compression and decompression, The video compression technique reduces the redundancy in the video data. To perform the video compression, the video frames are extracted from the given input video. The video frames are treated like an image whereas in each frame initially DWT transformation is applied. After the wavelet Transformation is applied to video frames, we obtained a compressed video. Figure 6 shows the video which is taking for compression. Let's say it is original video named 'shuttle.avi'.


**Fig 6 Original 'Shuttle' Video Frames**

The video frames are transformed into wavelet domain by DWT technique, and these video frames are reconstructed by IDWT technique, which are illustrated in fig.7. The parameters like size, duration, frame rate of original video and reconstructed video is same.

**Fig. 7 Reconstructed 'Shuttle' Video Frames**

For comparative study and further analysis, the algorithm can also be implemented in MATLAB 2013a with less computation. But drawback of designing algorithm in MATLAB is many of MATLAB code is not dump in FPGA. While using FPGA and MATLAB together it is somewhat complex.

## PERFORMANCE ANALYSIS

Our proposed video compression technique performance is tested with number of videos. Here, we have take single video for performing compression and decompression process by exploiting the proposed technique. The compression ratio, MSE and PSNR values are tabulated in the following table II. Our proposed video compression technique has given high quality compressed video than the different wavelet based compression method.

### *A. Compression Ratio*

The Compression ratio is defined as the ratio of size of uncompressed or Original video to the size of Compressed video. DWT method is used to achieve high compression ratio.

$$Compression\ Ratio = \frac{\text{Original Size}}{\text{Compress Size}}$$

### *B. Mean Square Error*

The Mean Square Error (MSE) is the cumulative squared error between the compressed and the original image. A lower value for MSE means lesser error.

$$MSE = \frac{1}{XY}\sum_{x=0}^{X-1}\sum_{y=0}^{Y-1}[f_{ij}(x,y) - f_{ij}^{'}(x,y)]^2 \quad (6)$$

Where $f_{ij}(x,y)$ are original video frames and $f_{ij}^{'}(x,y)$ is reconstructed video frames.

### *C. Peak Signal to Noise Ratio*

The Peak Signal to Noise Ratio (PSNR) is a measure of the peak error. Logically, a higher value of PSNR is good because it means that the ratio of Signal to Noise is higher. There is the inverse relation between the MSE and PSNR

$$PSNR = 10\log_{10}(255/\text{MSE}) \quad (7)$$

Where 255 is the maximum probable pixel value of the video frame.

**TABLE II: VIDEO COMPRESSION TECHNIQUE COMPRESSION RATIO, MSE AND PSNR VALUES**

| **Name of Video** | Shuttle.avi |
|---|---|
| **Compression Ratio** | 5.15 |
| **MSE** | 0.0029 |
| **PSNR** | 81.4539db |

**XPS Bus Interfaces**

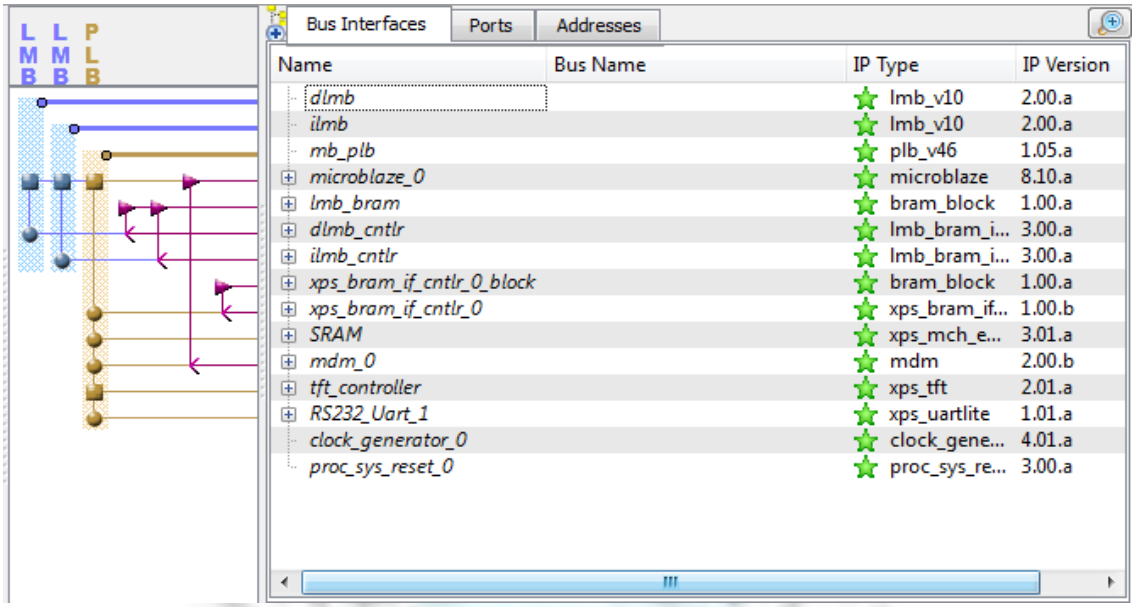


Fig. 8 XPS Bus Interfaces

## CONCLUSION

Managing the degree of difficulty to implement a design has always been a major consideration for video coding. Hence, compression of videos is necessary for transmission. In this paper, the architecture of 2D DWT is proposed which provides sufficient high compression ratio. DWT based video coding system is faster and requires less memory space than other methods. Wavelets are better suited to time-limited data and wavelet based compression technique maintains better image and video quality by reducing errors. Hence, our proposed video compression technique has offered better performance in compressing videos with higher compression ratio while maintaining desired video quality. The simulation results of DWT were verified with the appropriate test cases. The discrete wavelet transform is synthesized by using Xilinx tool in Virtex 5 FPGA family. Hence it has been analyzed that the discrete wavelet transform (DWT) operates at a maximum clock frequency. The XPS BUS Interface diagram shows that this design required minimum peripherals. This is also an advantage for video processing because of that power require and timing are less.

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