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Low Power High Speed Microprocessor using Q-Dot Devices

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ABSTRACT

Here we present a microprocessor which is similar to the existing ones except it consumes low power at very high clock. We develop the gates like AND/NAND, XOR, INV and D flip/flop based on oscillating charges/ions between two or more capacitors without getting dissipated in heat. We also made an adder based on these logic gates. These theoretical logic circuits are used to build the microprocessor.

1.0 INTRODUCTION

Digital microprocessor is used in desktop, laptop, tabloid, Smart Phone, Digital TV, washing machine, car and many other applications [1][2]. It is used round the clock. Here we present a novel approach in reducing the power consumption of microprocessor or the digital circuit associated with it. The origin of this idea has two basic approaches, one from differential CMOS digital gates [3] and other from, a basic Q-dot oscillator based circuit [4] which is the fastest. We convert them into the present form of pulsating dipole circuits using Q-dot devices.

The organization of this paper is as follows. The section I introduces the subject and the section II defines the differential logic gates based CMOS circuits, the starting point. The section III explains the Type-I logic gates using Q-Dot device. The section IV introduces the transmission gate topology. The section V deals with the Type –II gates. In the section VI we depict the single bit full adder circuit. In the section VII we conclude the paper.

2.0 DIFFERENTIAL LOGIC GATE USING CMOS

In the differential logic [3], the inputs and outputs are derived in true and complementary form in parallel. Thus AND/NAND gates are same and OR/NOR are similar to them. AND/NAND gate is explained in Figure 1 [2]. The top of the network is built using two pMOS transistors which feed dc voltage to the capacitor if the inputs are HIGH. Thus the output feeds current to the opposite capacitor making it HIGH, but itself will be LOW. Again if anyone of the inputs is LOW, the opposite output will be LOW, but itself will be HIGH.

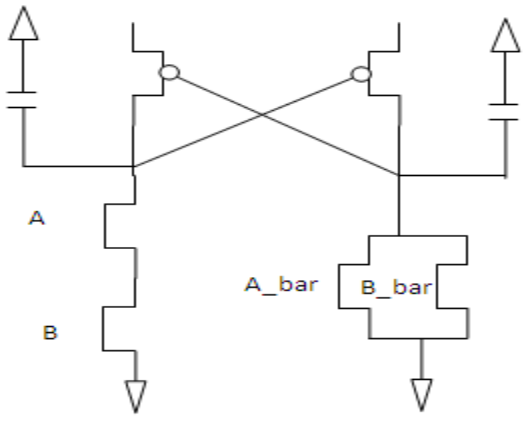

Figure 1. Differential logic gate for AND/NAND.

A differential D latch is shown in Figure 2 in CMOS technology. When the clock (CLK) is HIGH the output is LOW or H IGH depending on input A is LOW/HIGH which can be explained as in AND gate. It remains the same when CLK is LOW. The truth table is given in Table 1.

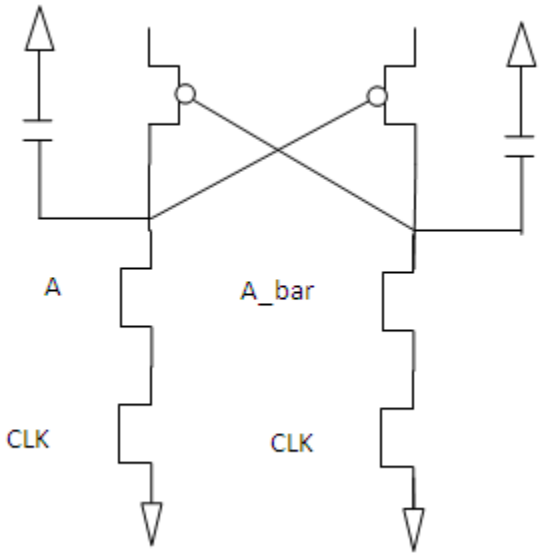

Figure 2. D latch

Table-I. D latch truth table.

INPUT	CLOCK	OUTPUT
HIGH	LOW	PREV
HIGH	HIGH	HIGH
LOW	LOW	PREV
LOW	HIGH	LOW

3.0 TYPE-I GATES

We can get a differential CMOS buffer as shown Figure 3, which we consider as an example for conversion to Q-dot circuit. If the CMOS gates in Figure 3, except the pull up transistors, are replaced by unidirectional Q-dot devices and the grounds are cross-coupled to the output capacitors we get a buffer shown in Figure 4. It gives a pulsating charge/ions depending on inputs which does not dissipate into heat.

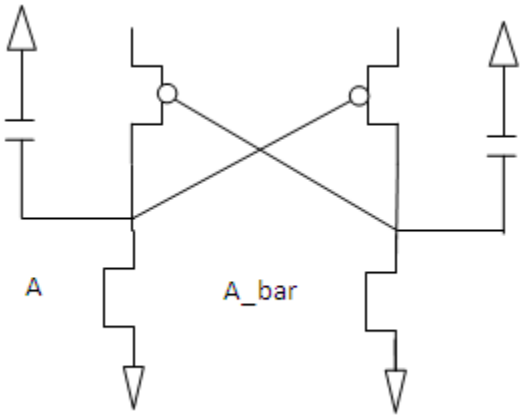

Figure 3. CMOS differential buffer.

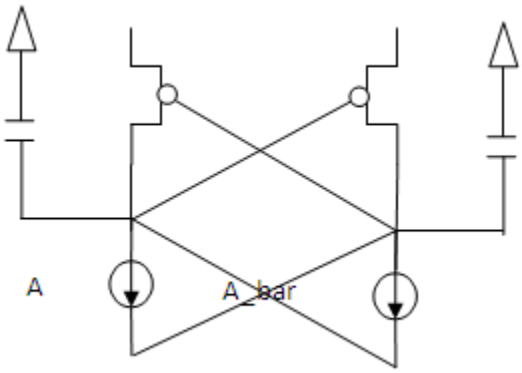

Figure 4. Q-dot differential buffer.

The D latch circuit is modified as shown in Figure 5. Similarly we can get AND/OR/XOR gates from the CMOS differential circuits.

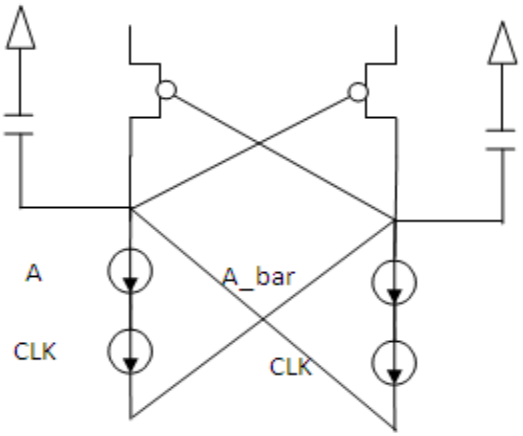

Figure 5. D Latch

4.0 TRANSMISSION GATE TOPOLOGY

The CMOS transmission gate topology is faster and easier to implement certain gates like AND, NOR and XOR and multiplexor/demultiplexor. The AND gate is shown in Figure 6. It is a signal is passed to a capacitor output. Hence the output will be HIGH if the input A is HIGH and the transmission gate is HIGH. The problem associated with it is that the capacitor needs to be leaky or has to be pulled down if the logical output is low. To do that we need differential output of AB and AB_bar. AB_bar is implemented by A_bar wired OR with B_bar. The complete circuit is shown in Figure 6. Similar modification is required for all other pass transistor based logic.

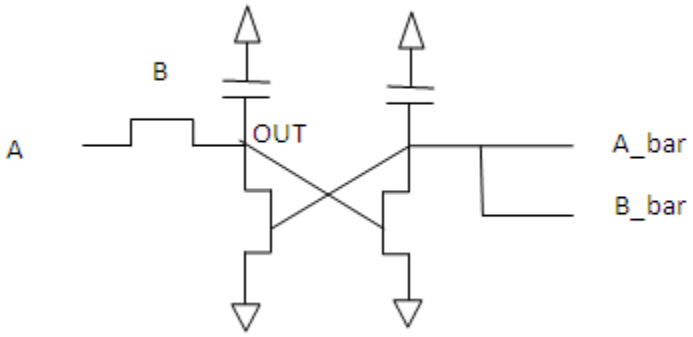

Figure 6. CMOS differential transmission gate topology for AND circuit.

5.0 TYPE-II GATES

The problem with Type-I gates are there are devices in series like in D latch. Hence, the data are to be synchronized all the time. A difference in timing will result in wrong output. We can avoid it by making it in two stages like in pass transistor logic in CMOS. We create a XOR gate. This is shown in Figure 7. We find that in the output stage there is a pull down circuit using a complementary logic circuit. Similar modification is done for AND gate as shown in Figure 8.

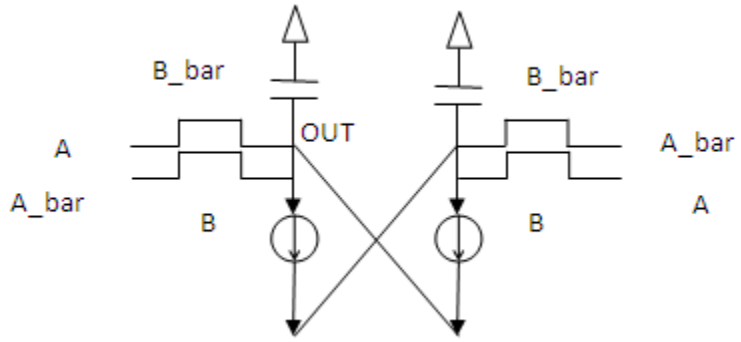

Figure 7. XOR gate

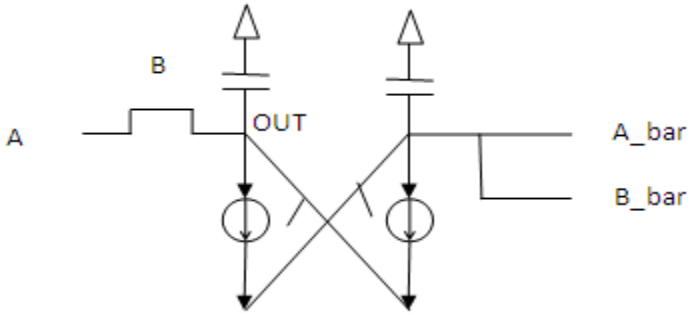

Figure 8. AND gate with pull down circuit.

6.0 ADDER

The adder circuit has two parts, one is the SUM (=A XOR B XOR C) and the other is CARRY(=AB+BC+CA). Like in CMOS pass transistor topology we require an active pull down circuit at the output and the pass transistors are represented by nMOS. Figure 9 and Figure 10 show the SUM and CARRY respectively. It is quite simple to balance the delay (of sum and carry) by putting an extra transistor in carry. We also can make them faster by implementing bidirectional device instead of nMOS pass gates.

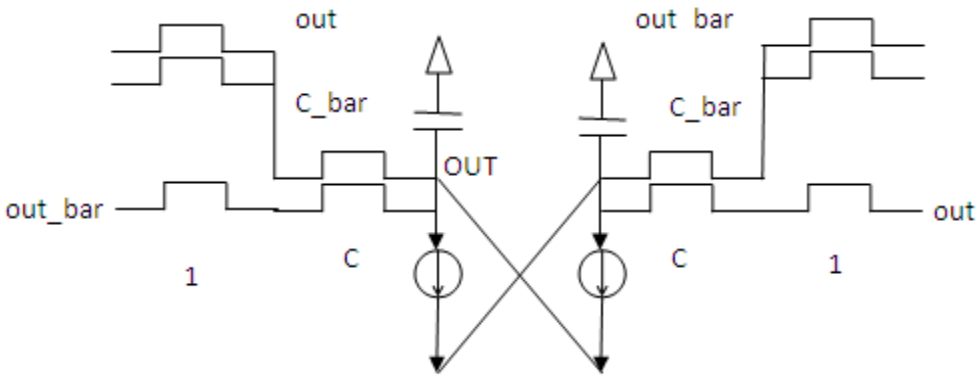

Figure 9. Sum of the adder.

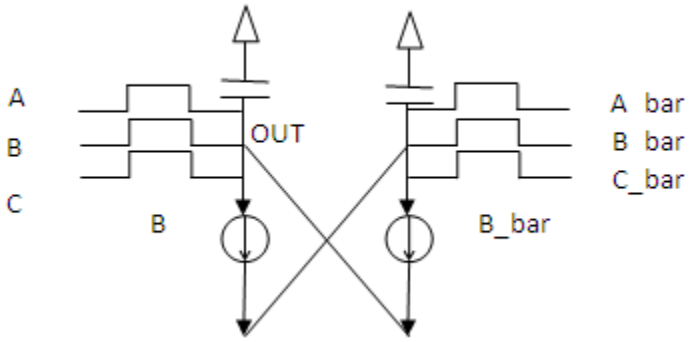

Figure 10. Carry of the adder.

The adder circuit in microprocessor is implemented as bit serial adder. The same technique is used to implement the multiplier which takes 72 clock cycles for 8 x 8 bit multiplier.

CONCLUSION

Microprocessor mainly consists of multiple (2 or 4) bit serial adders and multipliers. Here, we discuss possibility of adder and multiplier, starting from gate logic, to have low power loss. This allows the clock to be faster and a fastest microprocessor realization.

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