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Current Mode Logic Gates using Q-Dot Technology

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ABSTRACT: To design high speed computer we need high speed logic circuits. Here we present Q-dot technology based current mode logic gates which may satisfy that need. Also we introduce high frequency clock generation circuit and D latched based logic gates.

1.0 INTRODUCTION

Q-dot technology is touted as the next generation computer device. Normally Q-dot devices are used for Quantum Computer. But when the speed of computation is the criteria, the current mode logic gate gets preference in design.

Here we design a current mode oscillator charging and discharging in back to back fashion. This oscillator could be used for clock generation in Quantum computer. We can also use this circuit in frequency division and design of latched logic gates like OR, AND, XOR, MAJORITY, NOT and D flipflop.

Normally the voltage swing in high speed clock using the oscillator is in millivolt range and that will be the deciding factor in logic operation. The logic gates are made to operate at that voltage so that it can rum at that clock rate without failure. Noise will be the main problem in that low voltage. Hence we should not allow noise to accumulate and propagate. Thus we need circuitry to convert logic to rail to rail voltage operation, using a latch.

Section II introduces the circuit design for oscillator and Section III gives the design for logic circuits. This is extended in Section IV discusses the design for D latch and delay circuit. Section V illustrates the latched logic gates using OR and XOR as examples. Section VI concludes the paper.

2.0 OSCILLATOR

Two Q-dots can be connected in back to back fashion. The electron charge is taken from a capacitor (C1) so that the voltage across the capacitor will be higher. The charge is given to a capacitor (C2), so that its voltage will be lower.. Now the C1 lid will be connected to the gate voltage of Q-dot2 that is to Vg2 and the lid of C1 will be connected to the gate voltage of Q-dot1 that is to Vg1. Now as Vg2 is higher voltage then Q-dot2 will conduct and voltage across C2 will be higher and voltage across C1 will be lower. So Vg1 will be higher and at some point Q-dot1 will start conducting. This way Q-dot1 and Q-dot2 will conduct one after another. The voltage across the capacitance will pulsate at very high frequency across a bias voltage. The bias voltage is given from a dc source. At high frequency the lid from dc source behaves like an inductor and so there is no leakage of high frequency ac voltage. The frequency of oscillation depends on the value of capacitor and the current flow in the Q-dots. The oscillator circuit is shown in Figure 1. We can use the oscillator circuit as a clock generation circuit if its voltage swing is complete for every cycle.

3.0 LOGIC GATES

Here we design five current mode logic gates AND, OR, XOR, NOT and MAJority as shown in Figure 2. The Q-dot device is modeled as constant current source and the arrow shows the direction of electron flow. The device is biased at point L (at source) with a dc voltage. The signal will pulsate around the dc biasing point. The top current source works as the pull down logic and the bottom ones work as the logic generation.

In some of the logic generating branches like AND operation is done using series connected current sources. Their pulses have to be time synchronized. Complimentary logic design is also possible.

4.0 D-LATCH and DELAY CIRCUIT

There is a CMOS inverter based D-latch circuit as shown in Figure 3. The logic behind is implemented in Q-dot technology with a latch at the end. It is shown in Figure 4. Also a delay circuit is implemented as shown in Figure 5. based on the CMOS D latch.

5.0 LATCHED LOGIC GATES

Now we find that Vx depends on capacitor charging and discharging and the value of the capacitor. This depends on the process. So we put a SR latch which produces a rail to rail voltage variation with both the polarities at the same time. This is latched with CLK_bar signal. Thus we get a latched logic circuit. We have implemented OR and XOR with this logic as shown in Figure 6 and 7.

6.0 CONCLUSION

Here we developed digital circuits using Q-dot devices. We also implement D latch and delay circuit. We need to fabricate these circuits in laboratory and test their operating frequency.

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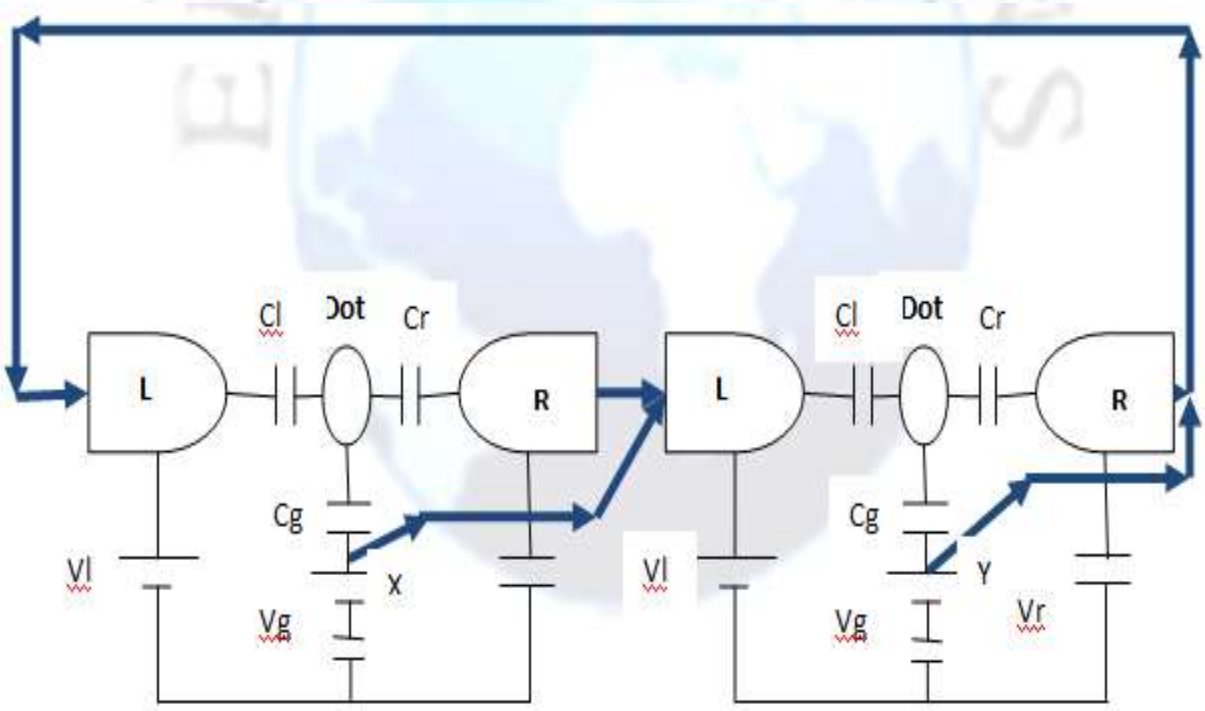

Figure 1. The oscillator circuit.

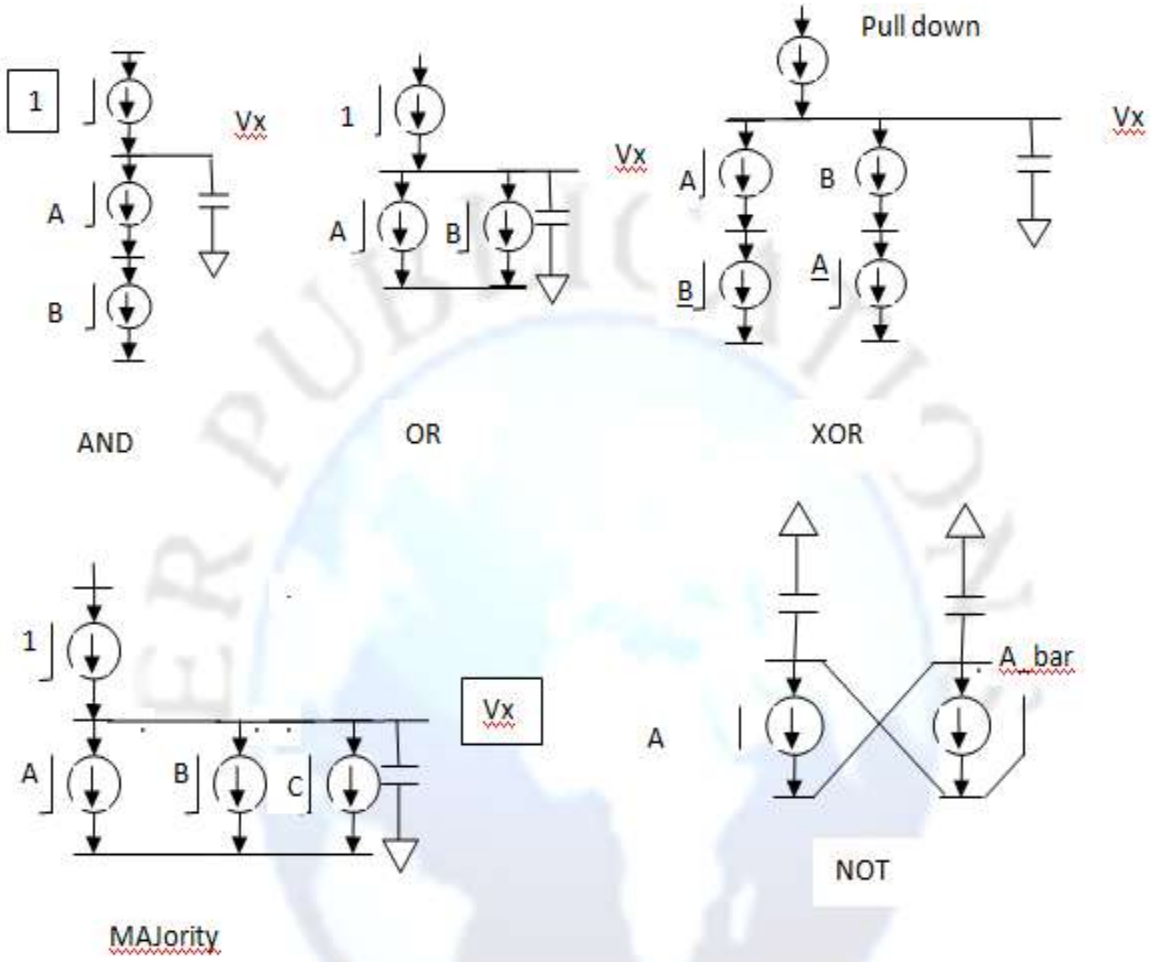

Figure 2. Different logic gates.

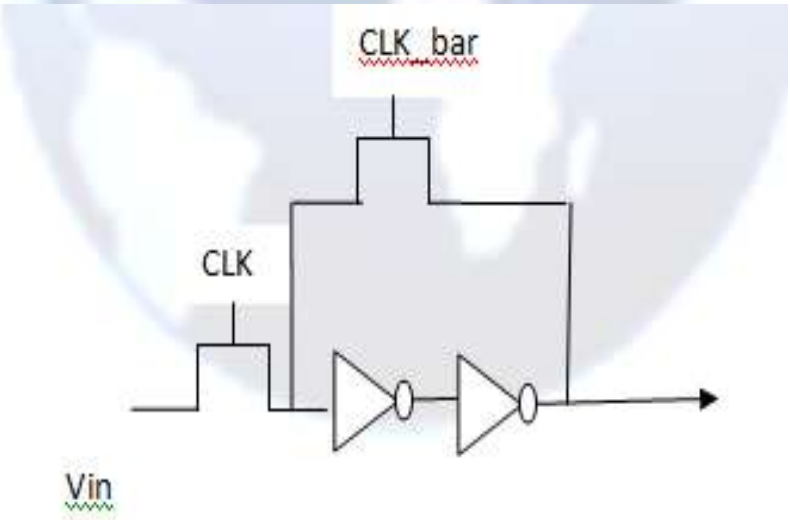

Figure 3. CMOS D-latch

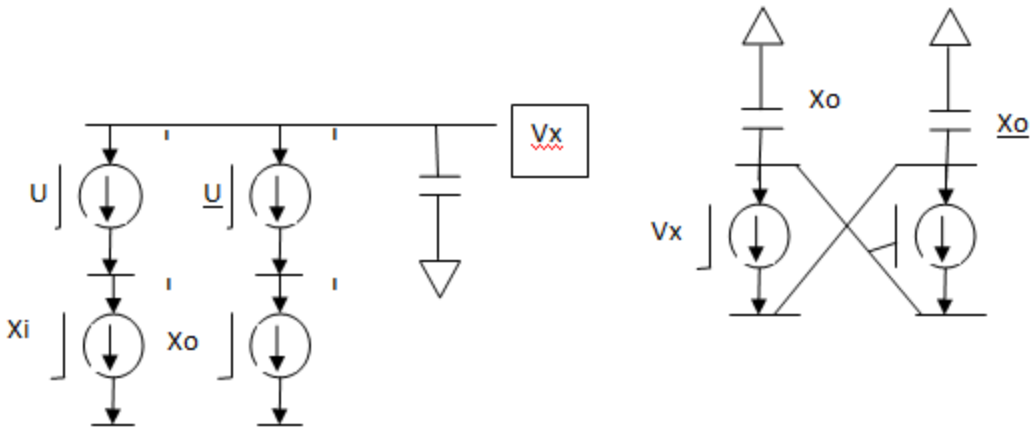

Figure 4. Q-dot D-latch

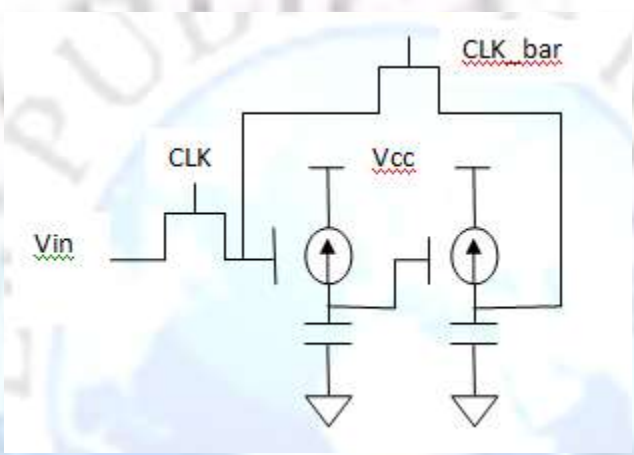

Figure 5. Delay circuit.

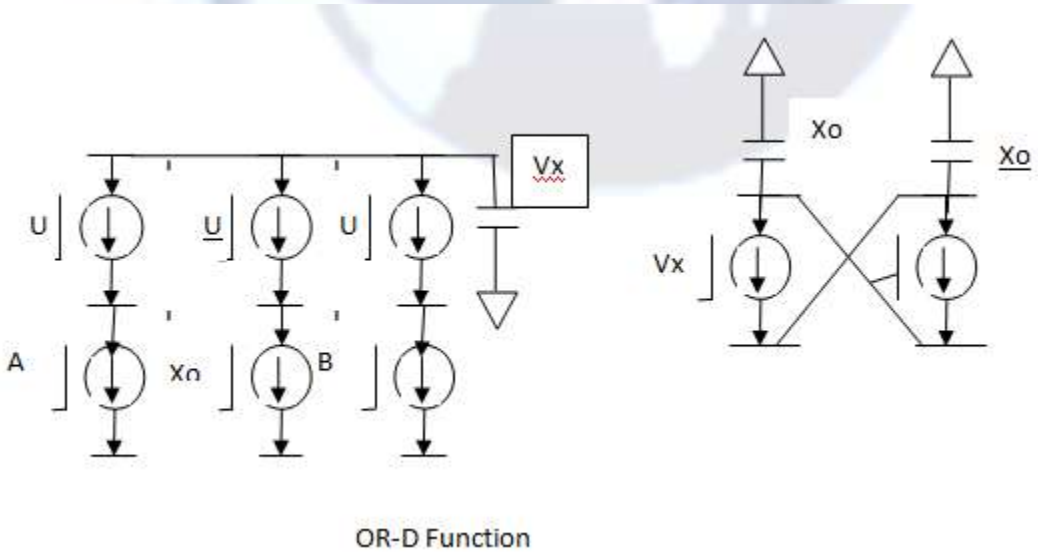

Figure 6. Latched logic function.

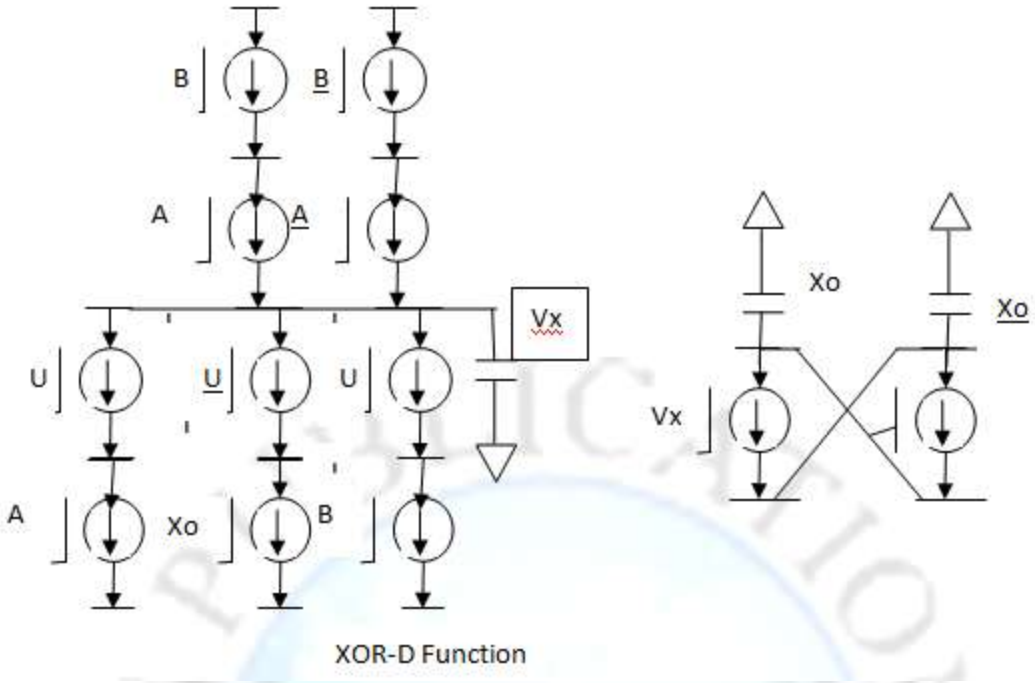

Figure 7. Latched XOR function