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Advanced Characterization of Analog Building Blocks

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ABSTRACT

This paper presents a new template-based tool for characterizing CMOS device models and basic analog building blocks using different technologies. The tool is based on simulations of built-in templates and measurements of the corresponding Figure-of-Merits (FOM) defined for each block that can be analyzed by the designer. The tool provides the designer a better insight into each block's operation by generating a detailed datasheet for the building block showing how different FOMs for each block vary with varying the corresponding bias conditions and/or device specs.

Keywords: Analog building blocks, MOS devices, technology characterization, Current Mirror, Differential Pair.

1. INTRODUCTION

Recent CMOS technologies are driven mainly by the digital market where the process is optimized for digital design and the devices are characterized for one main trade-off between speed and power dissipation. On the other hand, analog design is characterized by numerous device and circuit specifications [1]. This requires many design trade-offs between different specifications (e.g. gain, bandwidth, power and noise) and corresponding design parameters (e.g. transistor's length, width, bias voltage and currents) as shown in Fig. 1. Therefore, the design of analog circuits faces many difficulties due to poor characterization of devices.

Many CAD tools and environments have been proposed to facilitate and automate the characterization tasks to increase circuit quality and minimize effort and time. Most of those tools aim to provide the designer with the necessary characterization information through a set charts, plots or numerical look-up tables [2]. Our tool helps the designer with this time consuming technology characterization stage by automating the simulation of built-in testbenches for different CMOS devices or analog building blocks and generating a corresponding datasheet to use in the analog design flow giving more accurate circuit design and simulation results in less time.

The core of our tool is a Mentor Graphics tool called ICanalyst™ [3] that is responsible for running simulations required for characterization as well as generating datasheets.

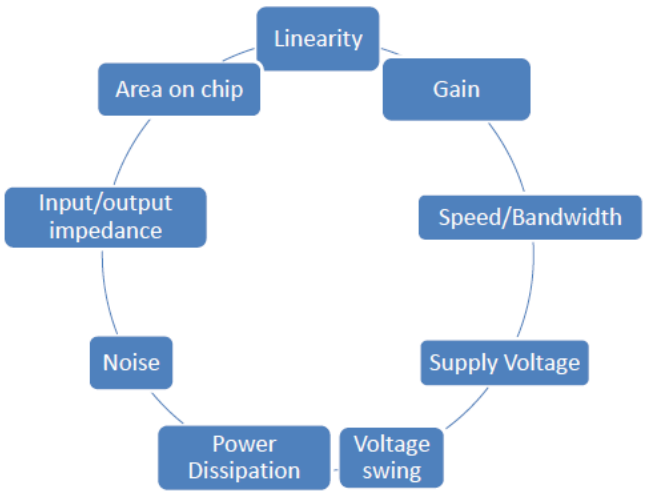

Figure 1. Analog circuits large specifications space

2. TOOL OVERVIEW

Our characterization tool demonstrates the importance of Tradeoffs in Analog IC design and how tradeoffs charts and information can be used in an efficient way. It allows the designer to explore visually the tradeoffs between important FOM's of MOS devices or analog IC basic building blocks and their relation with the corresponding devices sizing and biasing conditions [1], [2].

Our tool consists of a library of basic structures as shown in Fig. 2, which are:

a)	Nmos	e)	NCurrentMirror	i)	NDiffPair
b)	Pmos	f)	PCurrentMirror	j)	PDiffPair
c)	NCommonSource	g)	NCascodeCurrentMirror	k)	NCascodeDiffPair
d)	PCommonSource	h)	PCascodeCurrentMirror	l)	PCascodeDiffPair

The characterization capabilities of our tool allow the designer to change different parameters and observe the effect of these changes to performances of analog IC building block. The generated datasheets contain a wealth of information that the analog designer can use to determine the appropriate sizing of transistors in the circuit he designs. The charts and plots inside the datasheets also increase the understanding of tradeoffs in analog ICs and give more insight into the complex relationships between design parameters and performances of analog integrated circuits.

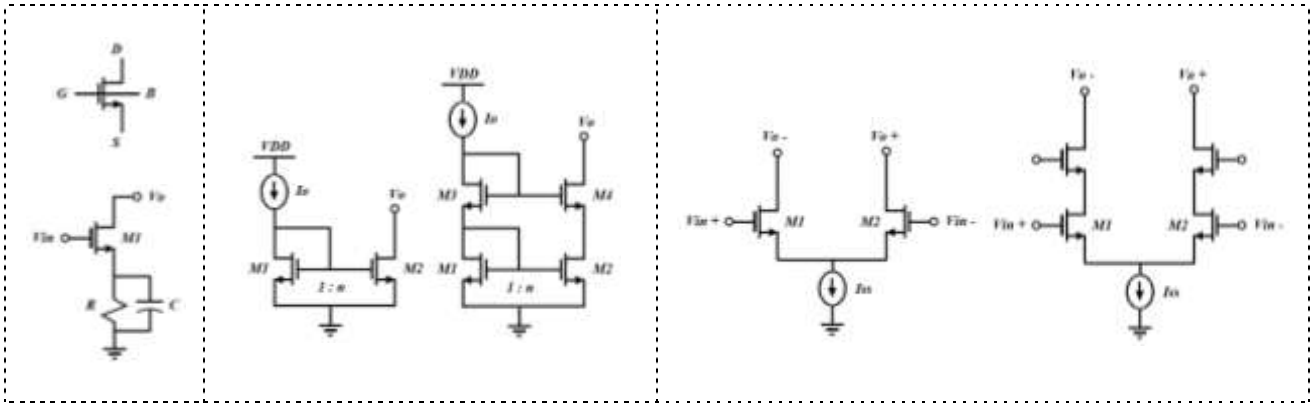

Figure 2. Analog building blocks library

3. BUILDING BLOCKS CHARACTERIZATION

A. Single Trasistor

The first building block to be characterized is the most elementary block in analog design which is the transistor, shown in Fig. 3. The transistor tradeoffs are very suitable in explaining the concept of our tool and how this concept is extended to more complex blocks. The important FOM's for the transistor [4], [5] are the transconductance efficiency (g_m/I_D), transit frequency (F_T), the intrinsic gain (g_m/g_{ds}) and current density (I_D/W).

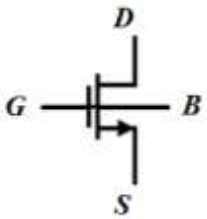

Figure 3. NMOS transistor

PARAMETERS TABLE

Name	Value	Source
temp	27.0	test bench
LN	From:0.06u To:2u Increment:0.2u	test bench
V2_VAL	.5500	test bench
V1_VAL	From:0.1 To:1.1 Increment:0.2	test bench

Figure 4. Inputs parameters for transistor characterization

The designer first enters ranges for sizing and biasing of the transistor, and then the tool automatically generates the datasheet containing charts and plots between the previously mentioned FOM's as well as numerical look-up tables. All the results are generated by the tool using 65nm technology. The next plots and numerical table are generated for the sweeps shown in Fig. 4, which represents the parameters table in the same format of the generated datasheet.

As an example, the output numerical look-up table for transistor characterization with the specified parameters is shown in Fig. 5 in the same format of the generated datasheet and a sample of tradeoff plots for transistor is shown in Figs 6 to 13 illustrating the variation of the important FOM's mentioned above versus transistor length and V_{GS} variations.

ALL CHARACTERISTICS TABLE

Test	FT	GM_GDS	GM_ID	ID_W	VDSAT	VOV	VTH	LN	V1_VAL
Test_1	1.19448e7	1.12394e1	2.73079e1	1.4463e-3	5.42137e-2	-4.539459e-1	5.539459e-1	6e-08	0.1
Test_2	2.0339e9	1.08142e1	2.43435e1	2.832856e-1	5.5121e-2	-2.5395e-1	5.5395e-1	6e-08	0.3
Test_3	3.88646e10	9.2154	1.38135e1	1.28988e1	8.24949e-2	-5.41318e-2	5.541318e-1	6e-08	0.5
Test_4	1.184501e11	7.5801	7.0615	9.11749e1	1.557882e-1	1.447393e-1	5.552607e-1	6e-08	0.7
Test_5	1.568961e11	5.4749	3.7285	2.387148e2	2.239771e-1	3.426079e-1	5.573921e-1	6e-08	0.9
Test_6	1.61576e11	3.6625	2.2882	4.068798e2	2.77527e-1	5.401729e-1	5.598271e-1	6e-08	1.1
Test_7	4.328361e5	5.42932e1	3.09349e1	8.46165e-5	5.06677e-2	-4.084426e-1	5.084426e-1	2.6e-07	0.1
Test_8	1.48228e8	5.23053e1	2.84017e1	3.57159e-2	5.14174e-2	-2.08443e-1	5.08443e-1	2.6e-07	0.3
Test_9	4.052e9	4.5162e1	1.62914e1	3.4078	9.16012e-2	-8.4836e-3	5.084836e-1	2.6e-07	0.5
Test_10	1.47545e10	3.29737e1	7.6191	3.24437e1	2.162597e-1	1.911673e-1	5.088327e-1	2.6e-07	0.7
Test_11	2.1868e10	1.631e1	4.0113	9.56443e1	3.52416e-1	3.904083e-1	5.095917e-1	2.6e-07	0.9
....	....	....	....	....	....	....	....	....	....
Test_49	5.53478e4	1.008397e2	3.13193e1	4.59899e-5	3.85074e-2	-3.407778e-1	4.407778e-1	1.66e-06	0.1
Test_50	1.07063e7	9.59339e1	2.68562e1	1.83405e-2	4.10847e-2	-1.40778e-1	4.40778e-1	1.66e-06	0.3
Test_51	1.654346e8	9.05724e1	1.38222e1	1.083	1.023657e-1	5.92082e-2	4.407918e-1	1.66e-06	0.5
Test_52	4.902248e8	7.05212e1	6.716	7.5222	2.407979e-1	2.591245e-1	4.408755e-1	1.66e-06	0.7
Test_53	7.56354e8	3.00283e1	3.8914	2.08107e1	4.066412e-1	4.589519e-1	4.410481e-1	1.66e-06	0.9
Test_54	7.568265e8	3.5722	2.2201	3.7879e1	5.885126e-1	6.587303e-1	4.412697e-1	1.66e-06	1.1
Test_55	4.82857e4	1.05281e2	3.13332e1	4.45623e-5	3.82256e-2	-3.360822e-1	4.360822e-1	1.86e-06	0.1
Test_56	8.9822e6	1.00109e2	2.67884e1	1.76897e-2	4.0999e-2	-1.360824e-1	4.360824e-1	1.86e-06	0.3
Test_57	1.366319e8	9.50959e1	1.3659e1	1.0201	1.041238e-1	6.39046e-2	4.360954e-1	1.86e-06	0.5
Test_58	3.968985e8	7.39381e1	6.637	6.9127	2.433379e-1	2.63828e-1	4.36172e-1	1.86e-06	0.7
Test_59	6.094977e8	3.05382e1	3.8619	1.89471e1	4.096215e-1	4.636717e-1	4.363283e-1	1.86e-06	0.9
Test_60	6.057307e8	3.5015	2.1997	3.43366e1	5.924451e-1	6.634718e-1	4.365282e-1	1.86e-06	1.1

Figure 5. Numerical Look-up Table for Transistor Characterization Results

A.1. Transconductance efficiency (gm/Id)

The first two plots illustrate the variation of transconductance efficiency (g_m/I_D) with the transistor's design parameters. Fig. 6 shows the relation between transconductance efficiency (g_m/I_D) and the transistor's length for different gate to source voltage (V_{GS}) values, while Fig. 7 shows the relation between transconductance efficiency (g_m/I_D) and the gate to source voltage (V_{GS}) for different values of transistor's length. The transconductance efficiency is the ratio between the MOSFET's transconductance (g_m) and drain current (I_D). It is a quality factor describing the production of desired transconductance for a given level of drain bias current. Theses plots are useful in determining the biasing of the transistor to give the required transconductance (g_m) for a certain drain current (I_D).

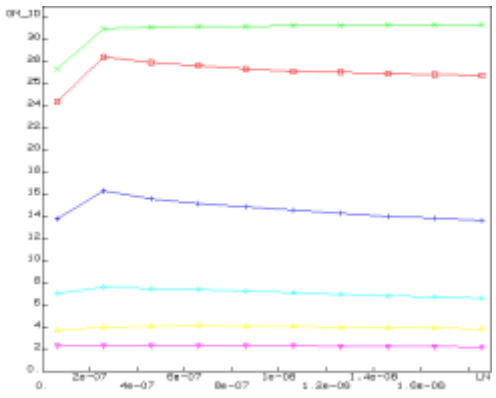

Figure 6. g_m/I_D vs L plot (for different V_{GS})

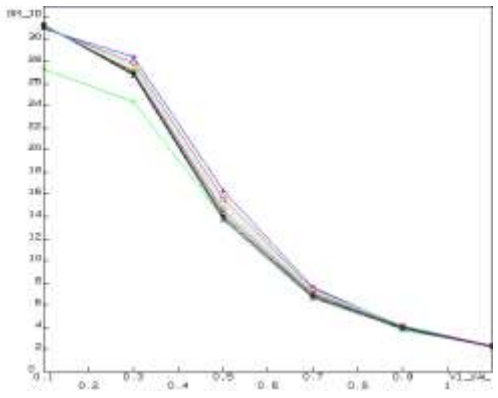

Figure 7. g_m/I_D vs V_{GS} plot (for different L)

A.2. Intrinsic gain (g_m/g_{ds})

The following two plots illustrate the variation of intrinsic gain (g_m/g_{ds}) with the transistor's design parameters. Fig. 8 shows the relation between intrinsic gain (g_m/g_{ds}) and the transistor's length for different gate to source voltage (V_{GS}) values, while Fig. 9 shows the relation between intrinsic gain (g_m/g_{ds}) and the gate to source voltage (V_{GS}) for different values of transistor's length. The intrinsic gain shows the maximum voltage gain that can be achieved from a single device. These plots show that more gain can be achieved from devices with longer lengths. This is due to the

increase in output resistance of the transistor ($R_{out} = 1/g_{ds}$) as the channel length increases. Also, the intrinsic gain plots together with the previous plots show that the intrinsic gain increases with the increase in transconductance efficiency.

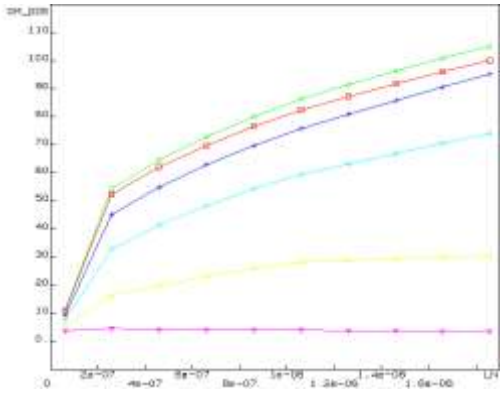

Figure 8. g_m/g_{ds} vs L plot (for different V_{GS})

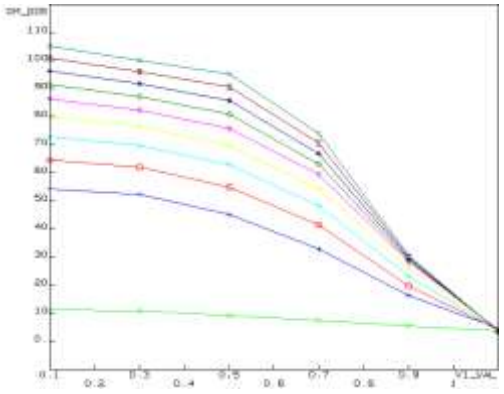

Figure 9. g_m/g_{ds} vs V_{GS} plot (for different L)

A.3. Current density (I_D/W)

The following two plots, shown in Fig. 10 and Fig. 11, illustrate the variation of current density (I_D/W) with the transistor's length and source to gate voltage respectively. These plots are used to determine the device width. After analyzing the above curves, the designer can choose a value for g_m/I_D, gate to source voltage (V_{GS}) and channel length to satisfy his specifications. Then the designer can determine the channel width by dividing the desired drain current (I_D) by I_D/W. These plots show that for a specific current and g_m/I_D, more width (more area) is needed to achieve this current for higher length devices. Also, other important information can be gained from this curve related to the previous chart of transit frequency.

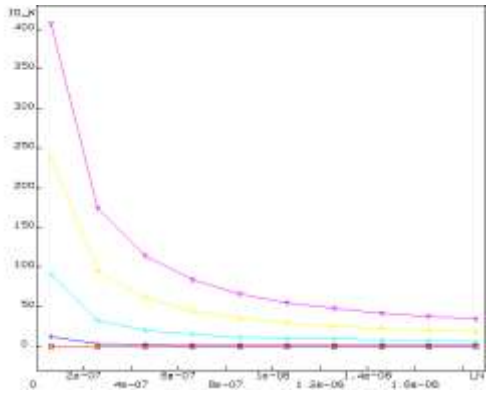

Figure 10. I_D/W vs L plot (for different V_{GS})

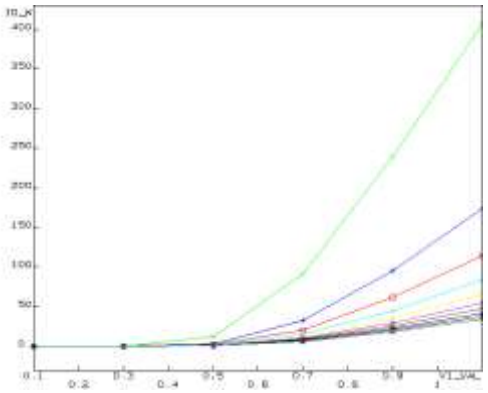

Figure 11. I_D/W vs V_{GS} plot (for different L)

A.4. Transit frequency (F_T)

The last two plots for the transistor, shown in Fig. 12 and Fig. 13, illustrate the variation of transit frequency (F_T) with the transistor's length and source to gate voltage respectively. The transit frequency equals g_m/C_{GG} which is the ratio between transconductance and parasitic capacitances. We want to maximize this ratio as possible since it means that the parasitic capacitance is low which lowers its effect in the overall circuit. It is also an important parameter that determines till which frequency the MOSFET can operate. The plots show that lower length devices achieve higher transit frequencies and the behavior approaches an inverse quadratic dependence between channel length and transit frequency.

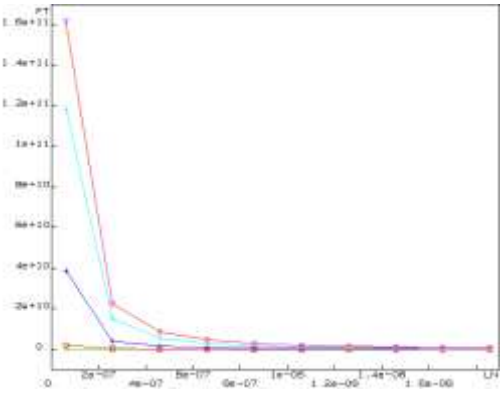

Figure 12. F_T vs L plot (for different V_{GS})

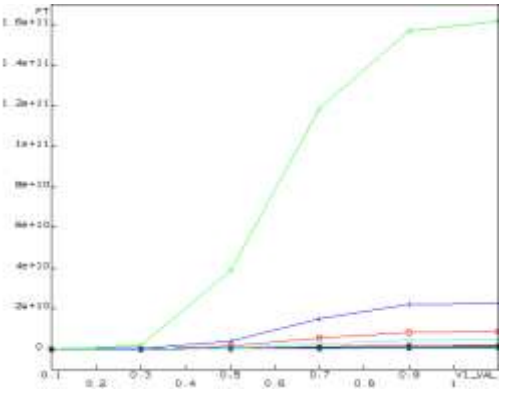

Figure 13. F_T vs V_{GS} plot (for different L)

B. Current Mirror

The current mirror is one of the most important building blocks in analog IC designs. Most of biasing in analog IC designs is done by current mirroring techniques. So, it is important to understand the tradeoffs found in the current mirror. The FOM's for current mirror [4], [5] are the transconductance efficiency (g_m/I_D), current ratio (I_{Ratio}), output impedance (R_{out}) and bandwidth (BW). The library of the tools includes both simple and cascode current mirrors where these blocks are characterized for NMOS and PMOS based designs. Fig. 14 shows the schematic of Simple Current Mirror to be characterized.

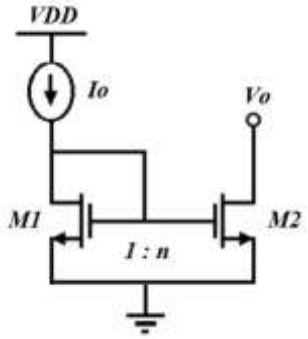

Figure 14. Simple Current Mirror

PARAMETERS TABLE

Name	Value	Source
temp	27.0	test bench
N	1	test bench
V2_VAL	.5500	test bench
I1_VAL	From:10u To:50u Increment:10u	test bench
LN	From:0.06u To:2u Increment:0.2u	test bench

Figure 15. Inputs parameters for simple current mirror characterization

The designer enters ranges for sizing and biasing of the transistors, the required current ratio and the required output DC voltage. Then the tool automatically generates datasheets with tradeoffs plots between the previously mentioned FOM's. All the results are generated by the tool using 65nm technology. The next plots and numerical table are generated for the sweeps shown in Fig. 15, which represents the parameters table in the same format of the generated datasheet.

As an example, the output numerical look-up table for simple current mirror characterization with the specified parameters is shown in Fig. 16 in the same format of the generated datasheet and a sample of tradeoff plots for simple current mirror is shown in Figs 17 to 24 illustrating the variation of the important FOM's mentioned above versus transistor length and reference current (I_o) variations.

ALL CHARACTERISTICS TABLE

Test	BW	GAIN	GM1	GM1_ID	GM2	GM2_ID	IIN	IOUT	IRATIO	ROUT	I1_VAL	LN
Test_1	4.9846e9	1.4099	1.975281e-4	1.97528e1	2.573209e-4	1.91206e1	1.e-5	1.34578e-5	1.3458	4.03878e4	1e-05	6e-08
Test_2	1.4016e9	3.54114e-2	1.82937e-4	1.82937e1	1.877979e-4	1.82028e1	1.e-5	1.0317e-5	1.0317	2.602646e5	1e-05	2.6e-07
Test_3	6.810476e8	-3.86619e-2	1.613554e-4	1.61356e1	1.635759e-4	1.60834e1	1.e-5	1.01705e-5	1.017	3.549141e5	1e-05	4.6e-07
Test_4	4.21289e8	-7.04226e-2	1.473494e-4	1.4735e1	1.484855e-4	1.47048e1	1.e-5	1.00977e-5	1.0098	4.408813e5	1e-05	6.6e-07
Test_5	2.94104e8	-8.64846e-2	1.370675e-4	1.37068e1	1.376451e-4	1.36901e1	1.e-5	1.00544e-5	1.0054	5.231473e5	1e-05	8.6e-07
Test_6	2.213067e8	-9.28589e-2	1.294515e-4	1.29452e1	1.297493e-4	1.29359e1	1.e-5	1.00302e-5	1.003	5.996663e5	1e-05	1.06e-06
Test_7	1.752478e8	-9.27435e-2	1.238911e-4	1.23892e1	1.240746e-4	1.2383e1	1.e-5	1.00198e-5	1.002	6.671937e5	1e-05	1.26e-06
Test_8	1.432354e8	-9.28997e-2	1.188557e-4	1.18856e1	1.189465e-4	1.18824e1	9.9999e-6	1.00103e-5	1.001	7.349234e5	1e-05	1.46e-06
Test_9	1.199219e8	-9.30034e-2	1.143156e-4	1.14316e1	1.143333e-4	1.1431e1	9.9999e-6	1.00021e-5	1.0002	8.025671e5	1e-05	1.66e-06
Test_10	1.023638e8	-9.29733e-2	1.102158e-4	1.10217e1	1.101764e-4	1.10232e1	9.9999e-6	9.995e-6	9.995053e-1	8.699489e5	1e-05	1.86e-06
Test_11	8.47e9	6.801339e-1	3.529085e-4	1.76454e1	4.230673e-4	1.71421e1	2.e-5	2.468e-5	1.234	2.38649e4	2e-05	6e-08
Test_12	2.2009e9	-9.5189e-2	3.136122e-4	1.56806e1	3.170587e-4	1.56403e1	2.e-5	2.02719e-5	1.0136	1.49487e5	2e-05	2.6e-07
....	....	....	....	....	....	....	....	....	....	....	....	....
Test_39	2.54646e8	-1.752599e-1	2.619975e-4	6.55	2.595854e-4	6.5702	3.99997e-5	3.95098e-5	9.877512e-1	2.903646e5	4e-05	1.66e-06
Test_40	2.14797e8	-1.718015e-1	2.486017e-4	6.2151	2.462952e-4	6.2334	3.99997e-5	3.95123e-5	9.878151e-1	3.132185e5	4e-05	1.86e-06
Test_41	1.62667e10	-1.819112e-1	7.32522e-4	1.46504e1	7.958315e-4	1.43928e1	5.e-5	5.52937e-5	1.1059	1.21547e4	5e-05	6e-08
Test_42	3.8888e9	-2.318373e-1	6.08348e-4	1.2167e1	6.05206e-4	1.21853e1	5.e-5	4.9667e-5	9.933395e-1	7.35466e4	5e-05	2.6e-07
Test_43	1.8365e9	-2.31244e-1	5.081289e-4	1.01626e1	5.035805e-4	1.01921e1	5.e-5	4.94089e-5	9.88178e-1	1.03381e5	5e-05	4.6e-07
Test_44	1.1067e9	-2.243096e-1	4.426883e-4	8.8538	4.38124e-4	8.885	4.99999e-5	4.93107e-5	9.862154e-1	1.308324e5	5e-05	6.6e-07
Test_45	7.533749e8	-2.163858e-1	3.954455e-4	7.9089	3.911408e-4	7.9387	4.99999e-5	4.927e-5	9.854019e-1	1.570023e5	5e-05	8.6e-07
Test_46	5.532551e8	-2.082198e-1	3.60227e-4	7.2046	3.562624e-4	7.2316	4.99999e-5	4.92646e-5	9.85294e-1	1.813263e5	5e-05	1.06e-06
Test_47	4.284424e8	-2.004731e-1	3.339745e-4	6.6795	3.303518e-4	6.7033	4.99998e-5	4.92818e-5	9.856396e-1	2.027854e5	5e-05	1.26e-06
Test_48	3.438501e8	-1.94927e-1	3.123034e-4	6.2461	3.089209e-4	6.267	4.99997e-5	4.9293e-5	9.858661e-1	2.229992e5	5e-05	1.46e-06
Test_49	2.834589e8	-1.909317e-1	2.94045e-4	5.8809	2.908387e-4	5.8992	4.99997e-5	4.93011e-5	9.860291e-1	2.417997e5	5e-05	1.66e-06
Test_50	2.386248e8	-1.881574e-1	2.783968e-4	5.568	2.753214e-4	5.5838	4.99996e-5	4.93072e-5	9.861521e-1	2.59004e5	5e-05	1.86e-06

Figure 16. Numerical Look-up Table for Simple Current Mirror Characterization Results

B.1. Transconductance efficiency (g_m/I_D)

The first two plots for the simple current mirror, shown in Fig. 17 and Fig. 18, illustrate the variation of transconductance efficiency (g_m/I_D) with the transistor's length and the reference current of the transistor M1 (I_o) respectively. These plots show that as current increases, the efficiency decreases. Also, the plots show that as the length increases, the transconductance efficiency decreases. This is due to the decrease in the W/L ratio, so an increase in the overdrive voltage of the transistor is required to achieve the same current.

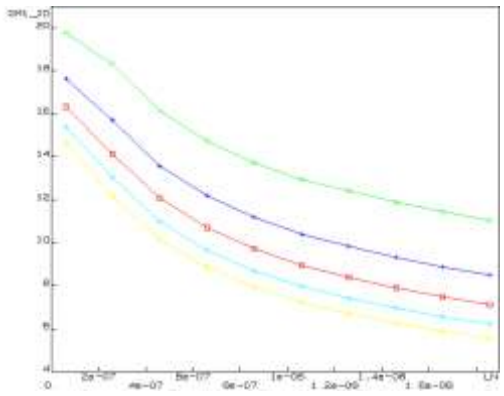

Figure 17. g_m/I_D vs L plot (for different I_o)

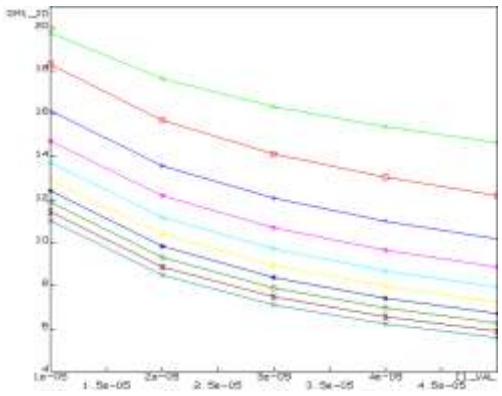

Figure 18. g_m/I_D vs I_o plot (for different L)

B.2. Current ratio

The following two plots illustrate the variation of the current ratio with the length of the current mirror transistors and the reference current (I_o) as shown in Fig. 19 and Fig. 20 respectively. These plots show that the current ratio deviates from the required current ratio. These deviations are due to channel length modulation effects. The current flowing in M2 depends on the drain to source voltage (V_{DS}) of this transistor. The drain to source voltage of M1 differs from that of M2, so large deviation is noticed. The plots also show that as the channel length increases, the current ratio approaches the required ratio.

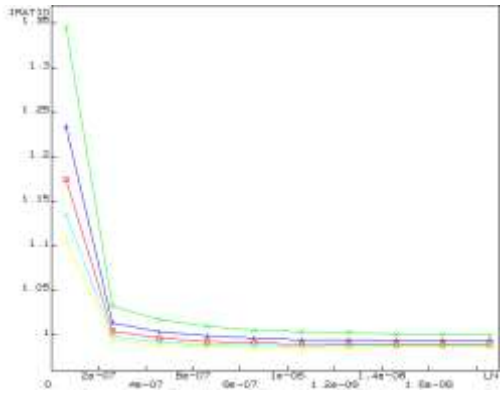

Figure 19. I_{Ratio} vs L plot (for different I_o)

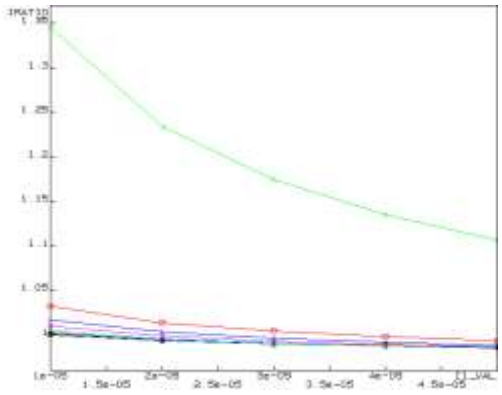

Figure 20. I_{Ratio} vs I_o plot (for different L)

B.3. Bandwidth

The following two plots illustrate the variation of the bandwidth with the transistors' length and the reference current (I_o) as shown in Fig. 21 and Fig. 22 respectively. The plots show that the bandwidth decreases with increasing channel length due to increasing parasitic capacitances.

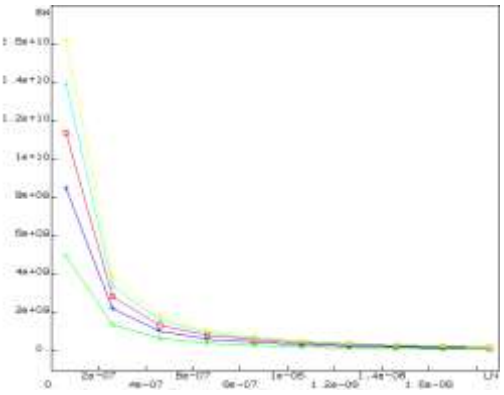

Figure 21. BW vs L plot (for different I_o)

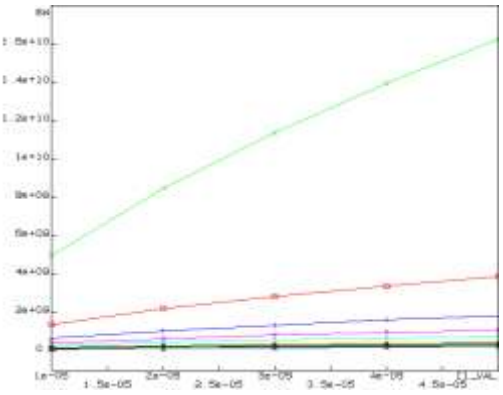

Figure 22. BW vs I_o plot (for different L)

B.4. Output impedance (R_{out})

The last two plots for the simple current mirror illustrate the variation of the output impedance (Rout) with the current mirror design parameters. Fig. 23 shows the relation between the output impedance and the current mirror transistors' length for different values of the reference current (Io), while Fig. 24 shows the relation between the output impedance and the reference current (Io) for different values of the transistors' length.

The output impedance Rout of the current mirror is given by:

$$R_{out} = {}^{1}/_{g_{ds|M2}} \cong {}^{1}/_{\lambda I_D}$$

These plots show that the output impedance (R_{out}) increases as the channel length increases due to the reduced effect of Channel Length Modulation (CLM). Also, from the plots, we observe that the output impedance increases (R_{out}) with decreasing current.

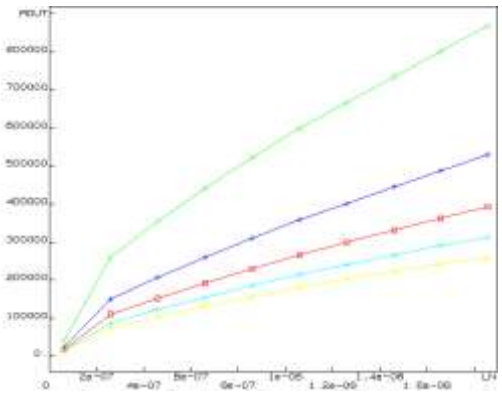

Figure 23. R_{out} vs L plot (for different I_o)

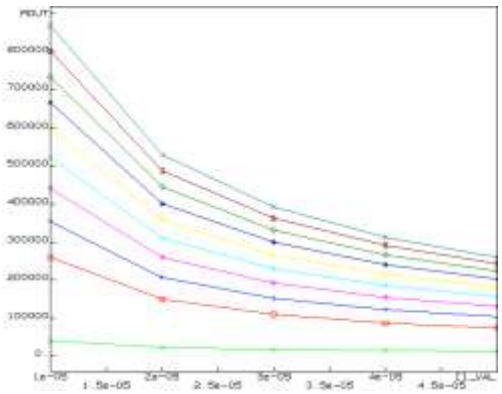

Figure 24. R_{out} vs I_o plot (for different L)

C. Differential Pair

Differential pairs are the basic building blocks of operational amplifiers. The library of the tools currently includes both simple and cascode differential pairs and these blocks are characterized for NMOS and PMOS based designs. The FOM's for the differential pair [4], [5] are the transconductance efficiency (g_m/I_D), differential gain, bandwidth (BW) and output impedance (R_{out}). Fig. 25 shows the schematic of Simple Differential Pair to be characterized.

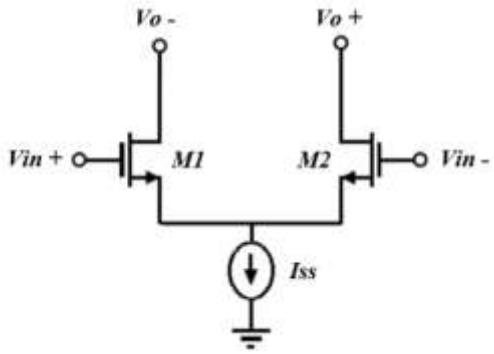

Figure 25. Simple Differential Pair

PARAMETERS TABLE

Name	Value	Source
temp	27.0	test bench
VIN_VAL	0.7	test bench
VO_VAL	0.7	test bench
I1_VAL	From:10u To:50u Increment:10u	test bench
LN	From:0.06u To:2u Increment:0.2u	test bench

Figure 26. Inputs parameters for simple differential pair characterization

The designer first specifies which effect of design parameters he wants to investigate (effect of transistor length or width). Next, He enters ranges for sizing and biasing of the transistors and the required output DC voltage. Then the tool automatically generates the datasheet containing plots between the previously mentioned FOM's as well as numerical look-up tables. All the results are generated by the tool using 65nm technology. The next plots and numerical table are generated for the sweeps shown in Fig. 26, which represents the parameters table in the same format of the generated datasheet.

As an example, the output numerical look-up table for simple differential pair characterization with the specified parameters is shown in Fig. 27 in the same format of the generated datasheet and a sample of tradeoff plots for simple current mirror is shown in Figs 28 to 35 illustrating the variation of the important FOM's mentioned above versus transistor length and bias current (I_o) variations.

ALL CHARACTERISTICS TABLE

Test	GM1	GM1_ID	GM2	GM2_ID	ROUT	I1_VAL	LN
Test_1	1.079569e-4	2.15914e1	1.079569e-4	2.15914e1	8.74039e4	1e-05	6e-08
Test_2	1.037341e-4	2.07468e1	1.037341e-4	2.07468e1	4.279252e5	1e-05	2.6e-07
Test_3	9.33444e-5	1.86689e1	9.33444e-5	1.86689e1	5.796525e5	1e-05	4.6e-07
Test_4	8.63577e-5	1.72716e1	8.63577e-5	1.72716e1	7.175193e5	1e-05	6.6e-07
Test_5	8.11925e-5	1.62385e1	8.11925e-5	1.62385e1	8.498859e5	1e-05	8.6e-07
Test_6	7.75312e-5	1.55063e1	7.75312e-5	1.55063e1	9.707532e5	1e-05	1.06e-06
Test_7	7.51336e-5	1.50268e1	7.51336e-5	1.50268e1	1.072e6	1e-05	1.26e-06
Test_8	7.2839e-5	1.45678e1	7.2839e-5	1.45678e1	1.1749e6	1e-05	1.46e-06
Test_9	7.06896e-5	1.4138e1	7.06896e-5	1.4138e1	1.279e6	1e-05	1.66e-06
Test_10	6.86923e-5	1.37385e1	6.86923e-5	1.37385e1	1.3838e6	1e-05	1.86e-06
Test_11	1.975295e-4	1.9753e1	1.975295e-4	1.9753e1	4.75508e4	2e-05	6e-08
....	....	....	....	....	....	....	....
Test_39	1.772681e-4	8.8634	1.772681e-4	8.8634	5.189551e5	4e-05	1.66e-06
Test_40	1.694929e-4	8.4747	1.694929e-4	8.4747	5.689231e5	4e-05	1.86e-06
Test_41	4.231903e-4	1.69276e1	4.231903e-4	1.69276e1	2.19635e4	5e-05	6e-08
Test_42	3.706821e-4	1.48273e1	3.706821e-4	1.48273e1	1.226262e5	5e-05	2.6e-07
Test_43	3.184022e-4	1.27361e1	3.184022e-4	1.27361e1	1.751547e5	5e-05	4.6e-07
Test_44	2.841892e-4	1.13676e1	2.841892e-4	1.13676e1	2.251889e5	5e-05	6.6e-07
Test_45	2.589589e-4	1.03584e1	2.589589e-4	1.03584e1	2.750733e5	5e-05	8.6e-07
Test_46	2.398048e-4	9.5922	2.398048e-4	9.5922	3.230684e5	5e-05	1.06e-06
Test_47	2.252498e-4	9.01	2.252498e-4	9.01	3.662253e5	5e-05	1.26e-06
Test_48	2.128285e-4	8.5132	2.128285e-4	8.5132	4.100484e5	5e-05	1.46e-06
Test_49	2.021048e-4	8.0842	2.021048e-4	8.0842	4.543503e5	5e-05	1.66e-06
Test_50	1.927419e-4	7.7097	1.927419e-4	7.7097	4.990034e5	5e-05	1.86e-06

(a)

BW	DIFFGAIN	GAIN
1.2551e9	1.30737e1	7.0531
7.835755e8	1.68797e1	1.08591e1
7.5121e8	1.63295e1	1.03089e1
7.327395e8	1.58591e1	9.8385
7.197102e8	1.54607e1	9.4401
7.094325e8	1.51538e1	9.1332
7.00292e8	1.49438e1	8.9232
6.919083e8	1.47277e1	8.7071
6.841223e8	1.45129e1	8.4923
6.768145e8	1.4303e1	8.2824
2.427e9	1.26357e1	6.6151
....	....	....
2.7359e9	1.06418e1	4.6212
2.7142e9	1.02815e1	4.2609
5.7445e9	1.18232e1	5.8026
3.7917e9	1.43526e1	8.332
3.6688e9	1.33431e1	7.3225
3.6025e9	1.25224e1	6.5018
3.5577e9	1.18229e1	5.8023
3.5222e9	1.12289e1	5.2083
3.4887e9	1.07352e1	4.7146
3.4593e9	1.0283e1	4.2624
3.4332e9	9.8671	3.8465
3.4095e9	9.4827	3.4621

(b)

Figure 27. Numerical Look-up Table for Simple Current Mirror Characterization Results
(a) DC OP Specifications (b) AC Specifications

C.1. Transconductance efficiency (g_m/I_D)

The first two plots for the simple differential pair illustrate the variation of the transconductance efficiency (g_m/I_D) with the differential pair design parameters. Fig. 28 shows the relation between the transconductance efficiency (g_m/I_D) and the differential pair transistors' length for different values of the bias current (I_o), while Fig. 29 shows the relation between the transconductance efficiency (g_m/I_D) and the bias current (I_o) for different values of the differential pair transistors' length.

The plots show that as current increases, the efficiency decreases (i.e. more power is consumed and less swing is achieved). Also, they show that as the length increases, the transconductance efficiency decreases. This is due to the decrease in the W/L ratio, so an increase in the overdrive voltage of the transistor is required to achieve the same current.

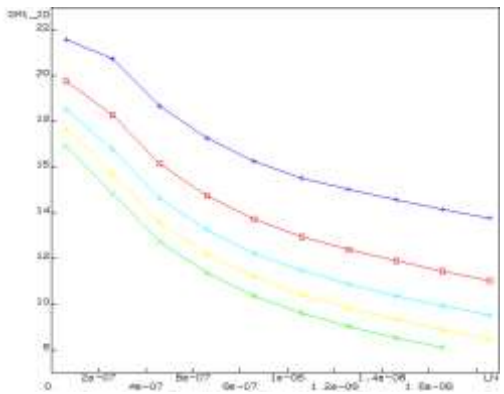

Figure 28. g_m/I_D vs L plot (for different I_o)

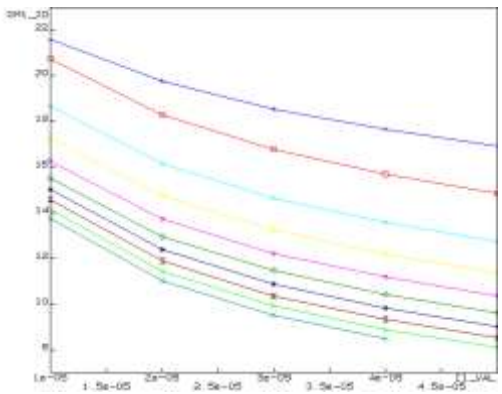

Figure 29. g_m/I_D vs I_o plot (for different L)

C.2. Output impedance (R_{out})

The following two plots illustrate the variation of the output impedance (R_{out}) with the differential pair transistors' length and the bias current (I_o) as shown in Fig. 30 and Fig. 31 respectively.

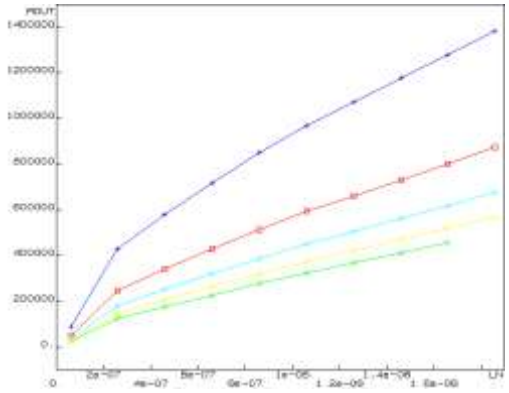

Figure 30. R_{out} vs L plot (for different I_o)

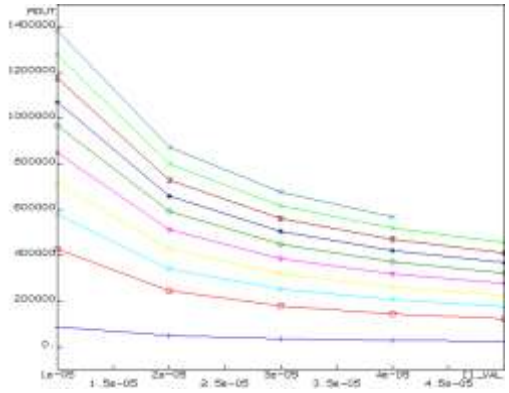

Figure 31. R_{out} vs I_o plot (for different L)

C.3. Differential gain

The following two plots for the simple differential pair illustrate the variation of the differential gain with the differential pair design parameters. Fig. 32 shows the relation between the differential gain and the differential pair transistors' length for different values of the bias current (Io), while Fig. 33 shows the relation between the differential gain and the bias current (Io) for different values of the differential pair transistors' length.

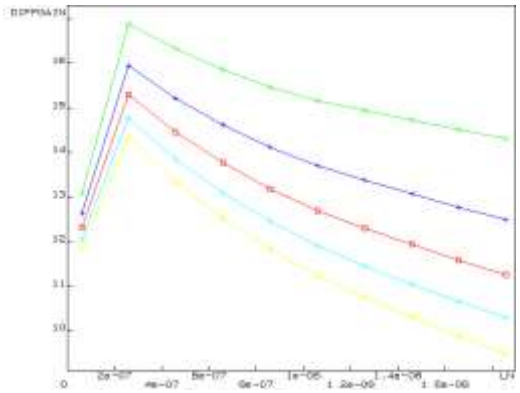

Figure 32. Differential Gain vs L plot (for different I_o)

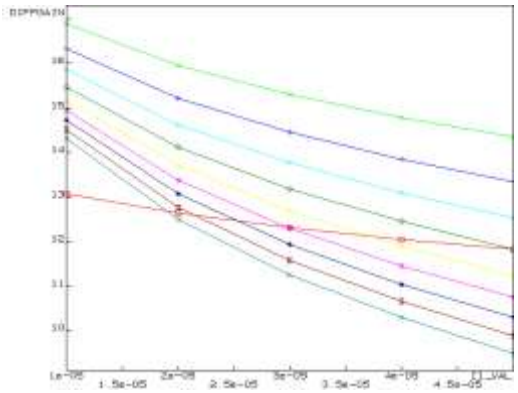

Figure 33. Differential Gain vs I_o plot (for different L)

C.4. Bandwidth

The following two plots for the simple differential pair illustrate the variation of the bandwidth with the differential pair design parameters. Fig. 34 shows the relation between the bandwidth and the differential pair transistors' length for different values of the bias current (I_o), while Fig. 35 shows the relation between the bandwidth and the bias current (I_o) for different values of the differential pair transistors' length.

We notice from the plots that as the channel length increases, the bandwidth of the simple differential pair decreases. This is due to the increase in the parasitic capacitances as devices dimensions increase. The plots also show that as the bias current (I_o) increases for a certain length, which means that the corresponding transconductance efficiency decreases, the bandwidth increases (a similar behavior to that of previous blocks).

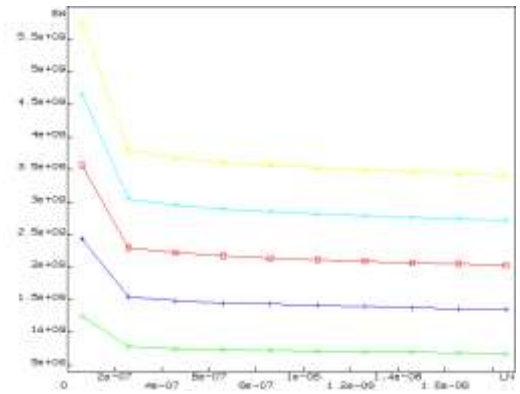

Figure 34. BW vs L plot (for different I_o)

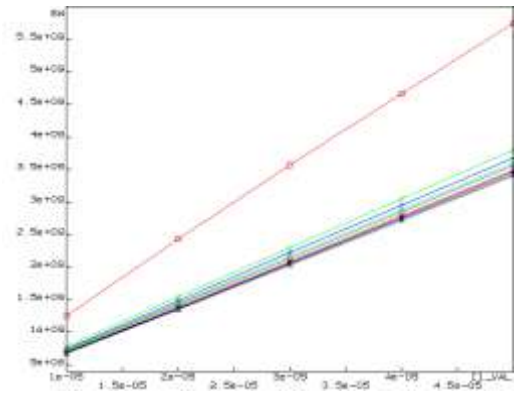

Figure 35. BW vs I_o plot (for different L)

4. CONCLUSION

This paper presented a new template-based tool that helps the designer characterize CMOS devices and analog basic building blocks and use the generated datasheet to get a better understanding of the concept of tradeoffs in analog IC design, the effects of changing different design parameters on circuit performance as well as the effects of different technologies and whether a certain technology can meet the specifications or not at an early design stage.

Also, in this paper, the contents of the generated datasheets such as plots and numerical look-up tables were presented for three main analog basic building blocks, which are; NMOS transistor, simple current mirror and simple differential pair using 65nm technology as examples of the beneficial usage of our tool's generated datasheets.

This tool can be extended to accommodate another operation mode that makes use of the current characterization capabilities of our tool, where it can automate the design flow of any analog circuit that can be divided into our supported analog basic building blocks by using the generated datasheets for optimizing those building blocks to achieve the analog circuit's required specifications.

REFERENCES

[1]. B. Razavi, "CMOS technology characterization for analog and RF design," IEEE J. Solid-State Circuits, vol. 34, pp. 268–276, Mar. 1999.
[2]. A. Hamza, A. Philip, M. Ali, M. Dessouky and M. Kassem, "Web-based analog design using tradeoff charts," ICECS, December 2012.
[3]. ICanalyst™, http://www.mentor.com/products/ic_nanometer_design/analog-mixed-signal-verification/icanalyst/
[4]. P. G. Jespers, The gm/ID Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits. Berlin, Germany: Springer, 2010.
[5]. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.