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10kHz, Low Power, 8th Order Elliptic Band-Pass Filter Employing CMOS VDTA

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Abstract: In this paper is presented a new active filter Voltage Differencing Transconductance Amplifiers (VDTAs) is presented. The active filter (VDTA) presented grounded inductance (GI) circuit and one grounded capacitor whereas the floating inductance (FI) circuit and one grounded capacitor. A series inductor and parallel capacitor through which realization of various active circuits is made by appropriate connections i.e. The proposed active and passive LC ladder filter is verified by realizing a 8th order band-pass elliptic filter using LTSPICE simulation with 0.18 µm TSMC CMOS technology parameters.

Keywords: VDTA, Inductance Simulation, LC ladder filters.

1. Introduction

The high order active filters can be realized by imitating the behavior of elements of LC ladder prototype filters and the approach for the designing of these filters has been already discussed in the literature [1, 10]**.** Many active elements were and are being proposed . Because there are important features relative to each other, such as input and/or output terminal can be different/same features, any parameter can be controlled by external voltage or current etc. New designs are provided for researchers with these new proposed active elements Presently, there is the interest of the availability of building active filters and other signal processing circuits without the use of physical coils. Although, a spiral inductor can be realized in an integrated circuit, it still has some drawbacks in the usage of space, weight, cost and tunability. The inductance simulators can be used in many applications such as active filter design, oscillator design, analog phase shifters and cancellation of parasitic element. The attention is subsequently focused on the inductance simulation using different high-performance active building blocks such as, Operational Transconductance Amplifiers (OTAs), current feedback op-amps, and four-terminal floating nullors (FTFNs), current conveyors, current differencing buffered amplifier (CDBAs), etc. The literature surveys shows that a large number of circuit realizations for floating and grounded inductance simulators have been reported. In this paper , we present novel floating simulators employing Differencing Transconductance Amplifier (VDTA), which is proven to be quite useful in eithercurrent or voltage-mode signal processing circuits. A new CMOS implementation of VDTA is given. The performance of the proposed circuit is tested with an application example of voltage-mode filter. By selecting input terminal voltages, this construction can generate the standard filter functions for voltage-mode. The proposed circuit employing minimum number of passive and active components uses external resistors and capacitors. Furthermore, no parameter matching condition is required[12, 13].

2. Experimental Investigation

2.1. VDBA Description.

The VDTA is a recently introduced active element which has two voltage inputs and two kinds of current output. The symbol of VDTA is shown in (Figure 1) and its CMOS implementation is shown in (Figure 2), where the input terminals are denoted as VP and VN and output terminals are Z, X+ and X−. The terminal relationship of VDTA can be described by the following set of equations:

$$\begin{bmatrix} i_z \\ i_{x+} \\ i_{x-} \end{bmatrix} = \begin{bmatrix} +g_{m1} & -g_{m1} & 0 \\ 0 & 0 & +g_{m2} \\ 0 & 0 & -g_{m2} \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_Z \end{bmatrix} \quad \text{.....(1)}$$

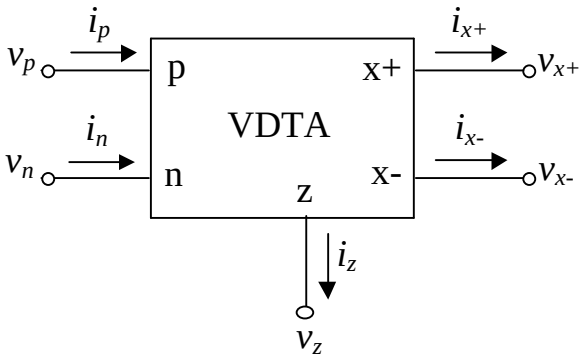

Figure 1. Symbol of VDTA

The input stage and output stage can be simply implemented by Improved floating current sources (I.F.C.S.). According to input terminals, anoutput current at Z terminal is generated. The intermediate voltage of Z terminal is converted to output currents. The new CMOS realization of the VDTA is shown in (Figure 2). The introduced circuit employs two Arbel - Goldminz transconductances. Input and output transconductance parameters of VDTA element in the circuit are determined by the transconductance of outputs transistors. It can be approximated [1] as :

$$g_{m1} = \frac{g_1 g_2}{g_1 + g_2} + \frac{g_3 g_4}{g_3 + g_4} \cong (g_{1,2} + g_{3,4})/2 \quad \text{.....(2a)}$$

$$g_{m2} = \frac{g_9 g_{10}}{g_9 + g_{10}} + \frac{g_{11} g_{12}}{g_{11} + g_{12}} \cong (g_{9,10} + g_{11,12})/2 \quad \text{.....(2b)}$$

where g_K is the transconductance value of K^{th} transistor defined by:

$$g_K = \sqrt{I_{BK}.\mu_K.Cox.\left[\frac{W}{L}\right]_k} \quad \text{.....(3)}$$

Where

$\mu_{K=}$ (K = n, p) the mobility of the carrier for NMOS (n) and PMOS (p) transistors.
C_{OX} = The gate-oxide capacitance per unit area.
W = The effective channel width.
L = The effective channel length.
$I_{BK=}$ Bias current of K^{th} transistor.

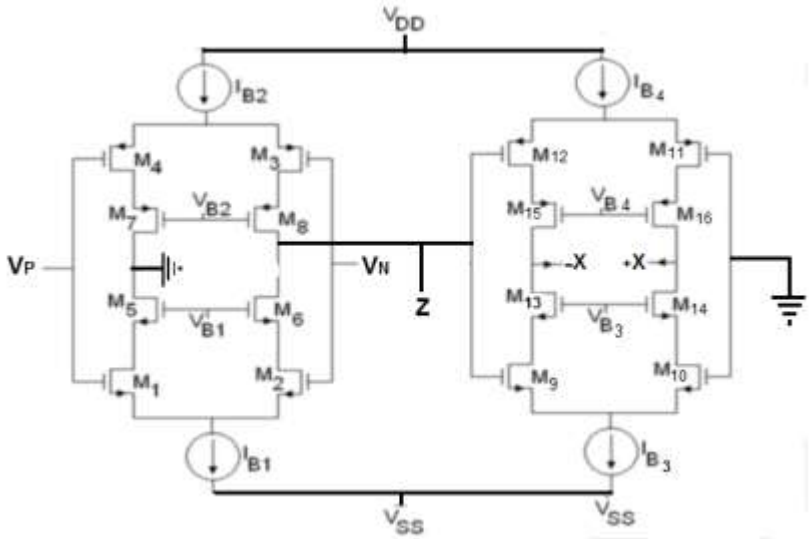

Figure 2. CMOS implementation of VDTA

2.2. Flouting and grounded inductor based on VDTA.

A flouting and grounded inductor which employ one of voltage differencing transconductance amplifier (VDTA) in(Figure 3) which contains Differential Input Single Output OTA (DISO) and Single Input Differential Output OTA (SIDO), and one grounded capacitor C_L.

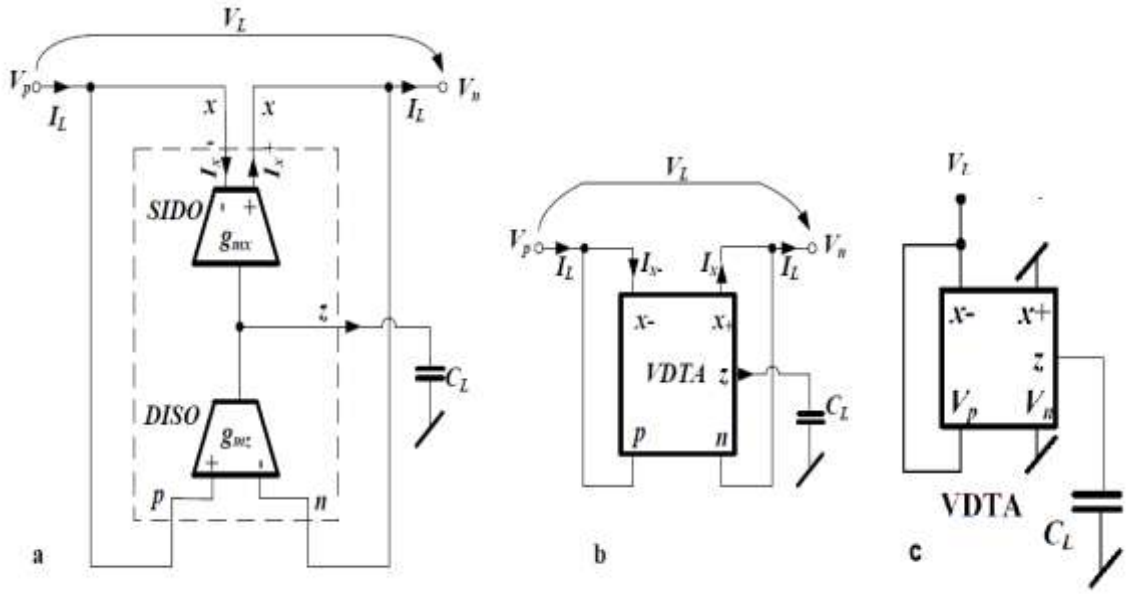

Figure 3. (a) Flouting inductor circuit employing DISO OTA and SIDO OTA, (b) Flouting inductor by VDTA, (c) Grounded inductor by VDTA

The process of transforming voltage difference (VP – Vn) into current Iz of DISO OTA is described by the equation:

$$Iz = gmz(Vp - Vn) \quad \text{.....(4)}$$

Current Iz causes voltage across the capacitor, and this voltage is transformed into current *I*x.

$$Vc = \frac{Iz}{SC_L} = \frac{g_{mz}(Vp - Vn)}{SC_L} \quad \text{.....(5)}$$

$$Ix = g_{mx}.Vc \quad \text{.....(6)}$$

$$Ix = g_{mx}.g_{mz}.\frac{(Vp - Vn)}{SC_L} \quad \text{.....(7)}$$

$$Zn = \frac{Ix}{(Vp - Vn)} = \frac{g_{mx}.g_{mz}}{SC_L} \quad \text{.....(8)}$$

The circuit, thus simulates a floating and grounded inductor with the resulting inductance given by :

$$L = \frac{g_{mx}.g_{mz}}{C_L} = \frac{g_m^{\,2}}{C_L} \quad \text{.....(9)}$$

(Figure 4) and (Figure5) shows that the magnitudes of the impedances of an ideal inductor with value equal to (47.1mH) which we used in LC ladder filter .The simulator circuit by voltage differencing transconductance amplifier (VDTA) as shown in (Figure 3) with *CL* equal to (3.85nF) can be made very close for a set of selected values over many decades.

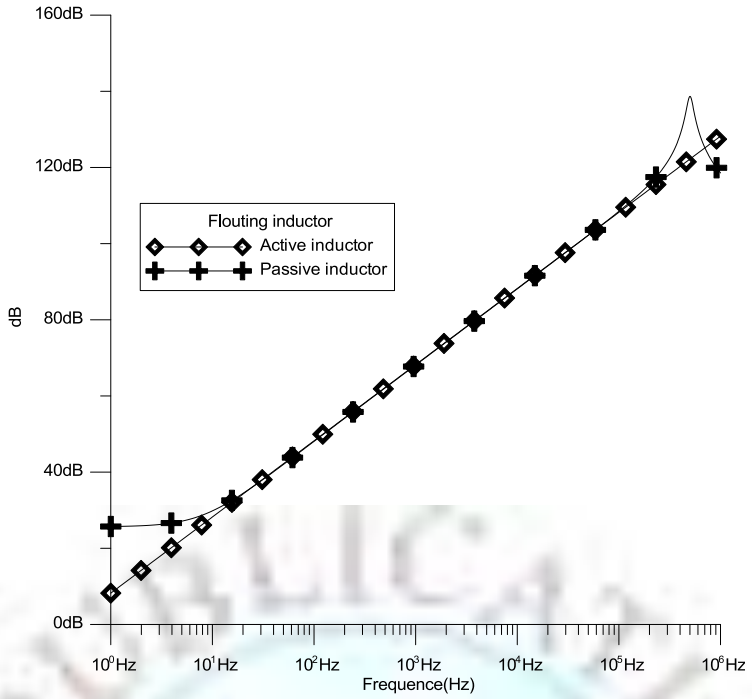

Figure 4: The impedance values relative to frequency of the ideal and simulated Flouting inductors.

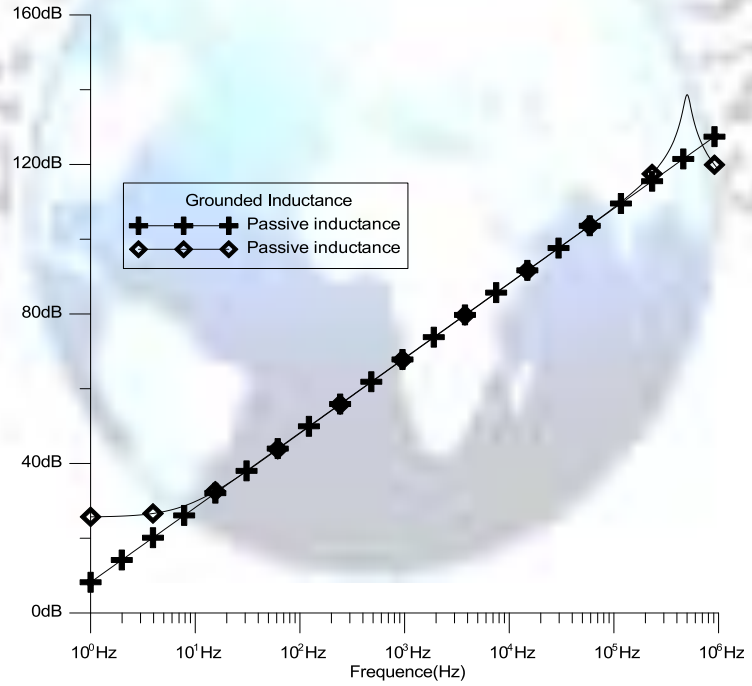

Figure 5: The impedance values relative to frequency of the ideal and simulated Grounded inductors.

3. Experimental Results and Discussion

The simulations by using LT. SPICE program with TSMC CMOS 0.18 μm process parameters are performed. The aspect ratios of the transistors are given in (Tab1). Supply voltages are taken as ($VDD = -VSS = 0.5$ V) and ($I_{B1} = I_{B2} = I_{B3} = I_{B4} = 8\mu A$) biasing currents are used. Simulation results show that this choice yields transconductance values of VDTA as ($g_{m1} = g_{m2} = 92.6$ μA/V). The DC transfer characteristic of I_{X+} and I_{X-} against V_Z for output stage of proposed VDTA is shown in (Figure 6). The DC transfer characteristic of input stage of VDTA is the same as I_{X+} of output stage.

Table 1.Transistors aspect ratios for the VDTA.

Device	W(µm)	L(µm)
$M_{1,9}$,$M_{2,10}$	18	0.18
$M_{3,11}$,$M_{4,12}$	72	0.18
$M_{7,15}$,$M_{8,16}$	90	0.18
$M_{5,13}$,$M_{6,14}$	27	0.18

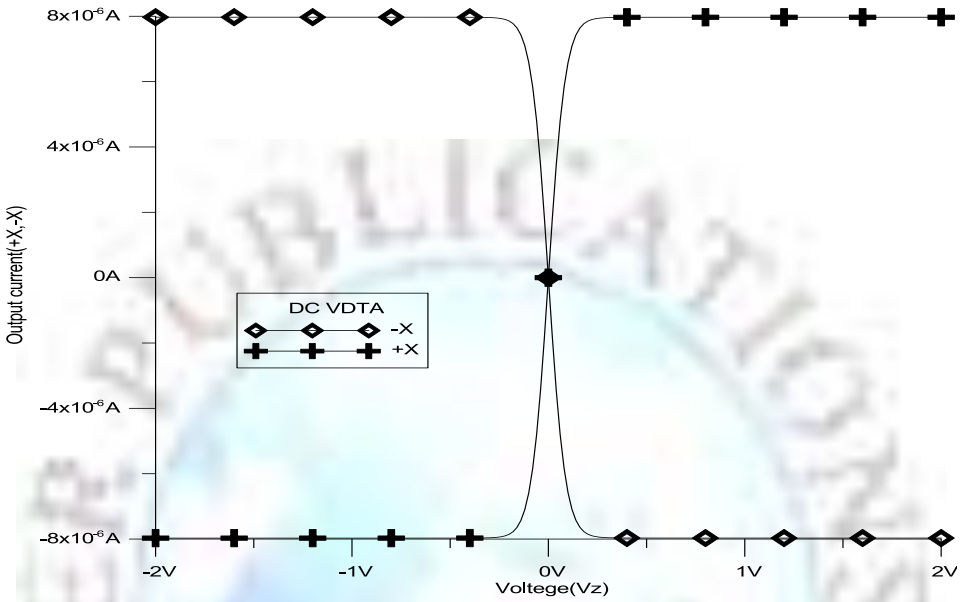

Figure 6.The DC transfer characteristic of the VDTA.

3.1. Band-pass 8th order elliptic LC Ladder simulation VDTA.

The schematic of 8th order a band-pass LC ladder filter shows in (Figure 7) which has been designed according to Cauer approximation on the basis of the following specifications: 8th order, central frequency equal to 10kHz, ripple 1dB, 60dB attenuation, The active simulation of the passive LC ladder filter from (Figure 7) by means of voltage differencing transconductance amplifier (VDTA) is given in (Figure 8). The floating and grounded inductor circuit in(Figure 3) with R_{load} equal to 10kΩ and the ladder filter component values are given in (Table 2).The active implementation of the filter component values and performance parameters are given in (Table 3).

Table 2. Ladder filter component values

Component	*Value Elliptic filter*
R1, R2	100KΩ
L1	0.41H
L2	43mH
L3	177mH
L4	679mH
L5	82.4mH
C1	616pF
C2	5.88nF
C3	372pF
C4	1.43nF
C5	3.07nF

Table 3: VDTA filter component values and performance parameters

Component	*Value Elliptic filter*
C_{L1}	3.85nF
C_{L2}	403.7pF
C_{L3}	1.662nF
C_{L4}	773.7pF
C_{L5}	773.7pF
G_M *Parameter*	
$g_{mz}=g_{mx}$	92.6 µA/V

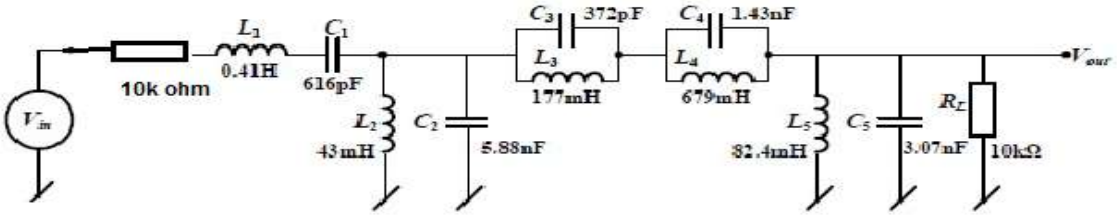

Figure 7. Band-pass 8th order elliptic passive LC Ladder filter

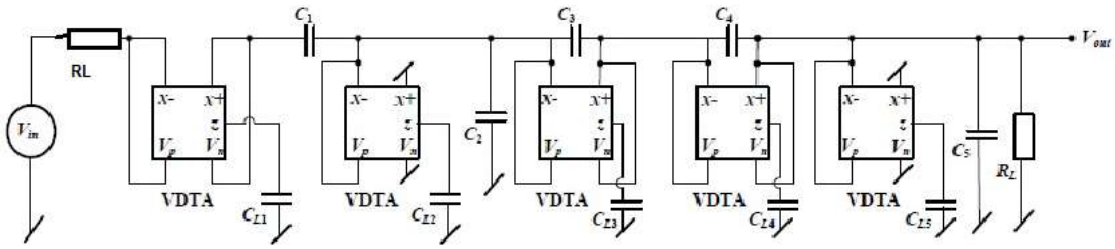

Figure 8. Active implementation for VDTA 8th order elliptic filter.

The frequency responses of the filter are shown in (Figure 9). It can be seen that the simulation using the true inductor and its VDTA simulators are in good agreement.

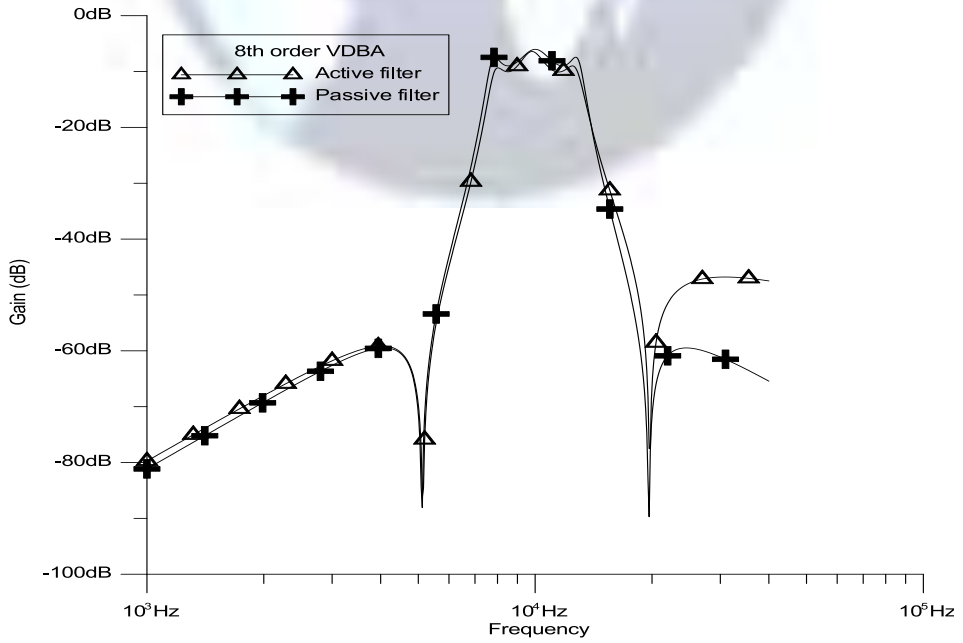

Figure 9. The frequency responses of ideal LC ladder and VDTA-based active filter

4. Conclusion

A new voltage differencing transconductance amplifier, VDTA is presented and implemented 8th order band-pass filter. A new and simple CMOS realization of this element is given frequency response of this filter for the VDTA is suitable for high frequency applications. Besides, since supply voltages are ±0.5V, the circuit is suitable for low voltage applications. An application example of a voltage-mode filter employing the proposed CMOS VDTA realization has been presented, since the proposed filter is constructed employing only a single active element, VDTA, where the value of transconductances can be adjusted by biasing currents. Simulation results that are simulated using LTSPICE confirm the theoretical results.

5. References

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