

A Novel Scheme to Reduce the Energy Consumption of Wireless Sensor Networks

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Abstract: Energy conservation in Wireless Sensor Networks (WSNs) has been a crucial issue, receiving increased attention in recent years. A novel interconnection scheme for energy-constrained WSNs is proposed in this paper. The scheme is about replacing the binary transceiver of the sensor node with a quaternary one. In particular, the link protocol will encompass amplitude/phase, modulator/demodulator units to increase the number of bits transmitted per symbol. This protocol allows transmission of code words more compactly, thereby reducing the energy needed for transmission.

Keywords: Demodulation, Modulation, Quaternary logic, Sensor networks.

I. INTRODUCTION

With the development of wireless sensor technology, transmission power of wireless sensor nodes is becoming a hot research topic. There is need to reduce network energy consumption in order to prolong node lifetime. There are so many approaches supposed to deal with such an issue. One such approach is compressive sensing [1], [2] which depends on compressing data before transmission and decompressing it upon reception. Another approach is clustering [3], [4], which divides the sensor network into a group of clusters with each cluster having a cluster head. The cluster heads then communicate with each other and transmit the available data to a base station which directly communicates with the server; however, all transmission protocols presented are based on a binary transmission scheme. In this scheme, one symbol carries only one bit. If we can make each symbol carry more than one bit, transmission will be more efficient, and therefore energy consumption will be lowered, and that is what this paper introduces. In other words, we will try to move from two-level logic to multi-level logic.

We propose to modify the design of sensor nodes so that each can deal with four symbols instead of two. Upon transmission each two bits will be modulated as one symbol, and upon reception the symbol will be demodulated producing the original bits. In section 2 symbol model is presented, section 3 presents the proposed scheme and the modulator/demodulator design, the performance is studied in section 4, and finally the conclusion is presented in section 5.

II. SYMBOL MODEL

Energy anatomy is widely recognized as one of the key challenges for monitoring infrastructures based on wireless sensor networks (WSNs) [5]. Several approaches have focused on WSN-based monitoring [6]. Technology oriented approaches design new circuits and systems for more efficient scheduling and transmission protocols. They try to bridge the gap between data sensing and transmission requirements and the corresponding energy harvesting and storage capability of the underlying hardware.

The advantage of multi-valued logic (MVL) is that it can execute arithmetic functions faster, using fewer interconnections. In addition, non-binary data transmission power becomes less because the number of the coded words will be fewer.

The concept of drawing the constellation diagram can be easily realized. The fact that 2 bits can represent the quaternary QAM means that one bit identifies the phase shift and the second one identifies the amplitude shift, thus allowing having a lower number of amplitudes and reducing the number of error probabilities. Table 1 shows the truth table of the system.

As seen in the proposed quaternary constellation diagram (Figure 1) each frame represents a state (amplitude) and each axis represents two states (the positive values are assigned to one state and the negative to the second one).

Table 1: 4-QAM in Quaternary

PSK	ASK	Overall
0	0	present in figure3
	1	present in figure3
1	0	present in figure3
	1	present in figure3

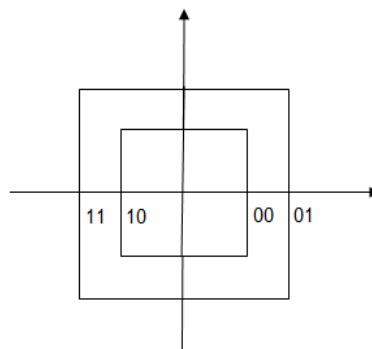


Figure 1: Quaternary constellation diagram

III. PROPOSED SCHEME

The solutions found in the literature for converting a binary interconnecting link into a quaternary one are composed of two parts: a binary-to-quaternary modulator and a quaternary-to-binary demodulator. A basic description of the link is shown in Figure 2.

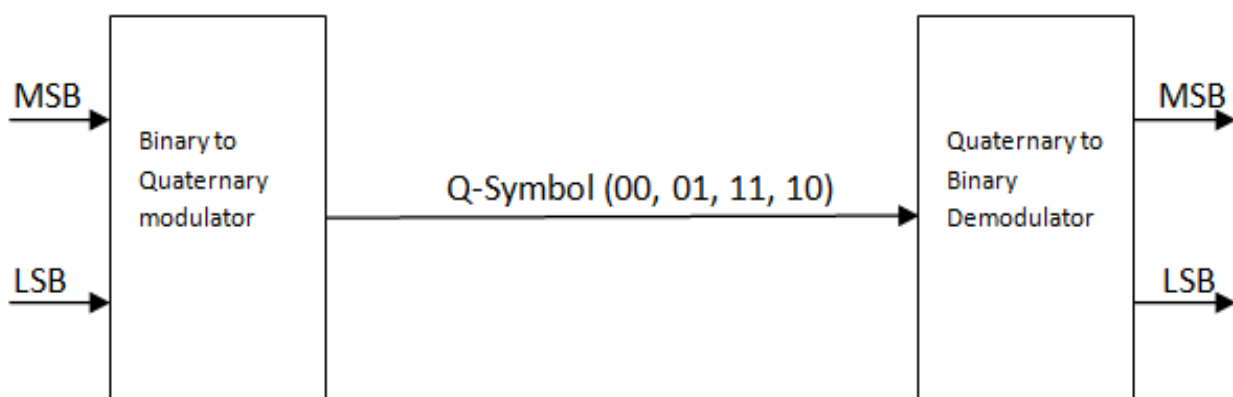


Figure 2: Structure of the proposed link

A. Link Basic Elements

The Quaternary link consists of a modulator and a demodulator. The power supply used in both modulator/demodulator circuits is 1.2 volt, where the wires used are 0.13≠m.

B. Transmission/Reception

a. Transmission

When a symbol of k bits arrives to the transmitter of a sensor node, this latter detects them and converts them into a symbol composed of a set of quaternary digits. For the corresponding symbol signal to be generated; this signal has a specified amplitude and phase shift combination.

The transmitted waveform is given by equation 1:

$$Q_0(x) = \sqrt{E_r[\cos(\theta_r)\phi_1(t) - \sin(\theta_r)\phi_2(t)]} \quad \text{Eq. (1)}$$

Where:

$$\phi_1(t) = \sqrt{\frac{2}{T}} * \cos(\omega_c t) \quad \text{Eq. (2)}$$

$$\phi_2(t) = \sqrt{\frac{2}{T}} * \sin(\omega_c t) \quad \text{Eq. (3)}$$

The design of the modulator used in the scheme is shown in Figure 3. This circuit converts each binary two bit symbol into a quaternary symbol.

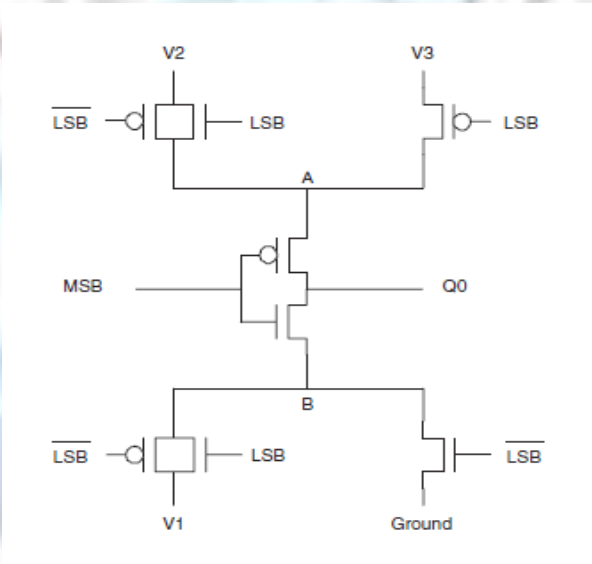


Figure 3: Binary to Quaternary Modulator design

The binary inputs of the modulator are the outputs of a sensor node, each modulator has two inputs one for the least significant bit (LSB) and the other for the most significant one (MSB) with one output denoted by Q0. Q0 is the quaternary symbol to be transmitted over the network from a sensor node to a base station, then from a base station to the designated server. We use the coding scheme presented in Table 2 where 0, 1, 2 and 3 are considered to be the four logic levels to be transmitted using the proposed quaternary link.

Table 2: Binary to quaternary modulating

MSB	LSB	Q0
0	0	3
0	1	2
1	0	1
1	1	0

First the amplitude of the received signal is determined and checked out. Then, the phase shift is estimated and checked, after being mapped on the constellation diagram, there may be two amplitude possibilities:

- **Case 1**

If $\sqrt{E_r} \leq \frac{(\sqrt{E_0} + \sqrt{E_1})}{2}$; then the signal is located within the right track; it could be one of two possible symbols (00, 01).

- **Case 2**

If $\sqrt{E_r} > \frac{\sqrt{E_0} + \sqrt{E_1}}{2}$; then the signal is located within the left track; it could be (10, 11).

At the end, a phase shift check is realized by looking it up in the phase shift table (Table 2).

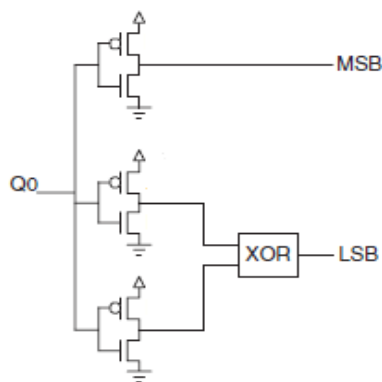


Figure 4: Quaternary to binary demodulator design

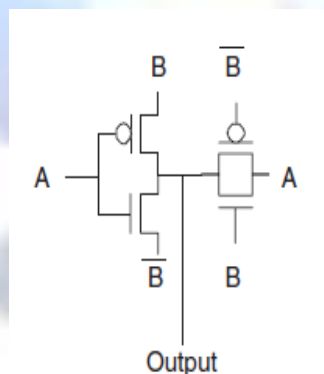


Figure 5: XOR gate design

b. Reception

The primary process in the reception stage of the communication system is the demodulation. The quaternary link transmits the quaternary symbol from the source sensor node (generated by the modulator) to the destination where it is received by the demodulator. The outputs of the demodulator are the inputs of the base station. As shown in Figure 4, the quaternary to binary demodulator used in our study is composed of three modified inverters whose inputs are the quaternary symbols, and an XOR gate (Figure 5).

The quaternary to binary demodulator (Figure 4) is composed of 12 transistors using the same power supply of the modulator. The Q0 quaternary signals arriving drives the bank of inverters, which in turn permits the isolation of the four quaternary digits to reform the binary symbol originally sent by the sensor node.

IV. PERFORMANCE

In order to assess the feasibility of the proposed scheme, we have simulated it using SPICE. Converting the symbols from binary to quaternary will shorten the symbol rate on the link, thus saving power and prolonging the wireless sensor network life time. In the simulation, we have adjusted the fall and rise time to be 0.1 ns for all the transitions. The simulation result of the binary to quaternary modulator is shown in figure 6, while that of quaternary to binary demodulator is shown in figure 7. Simulations had shown that the proposed quaternary signaling scheme reduces up to 41% of power consumption in a sensor node as shown in Figure 8. Also, since the simulation is done at 500 MHz, this means that the scheme will be stable for high-speed links.

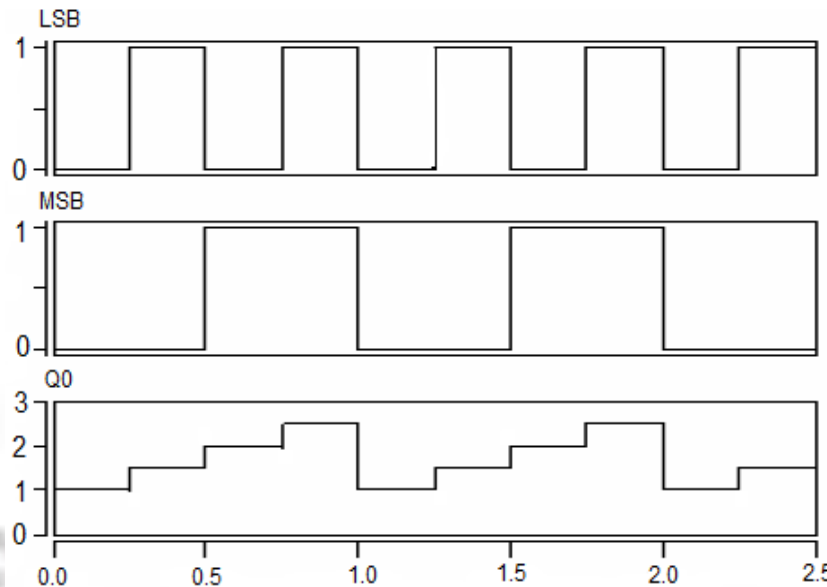


Figure 6: Binary to quaternary modulator simulation

Comparing the proposed quaternary link scheme with binary structures (choosing the least significant bit and the most significant bit randomly) to measure the energy consumption, it is found that the link is saving 41% of energy consumption. The energy consumption is shown in detail in Figure 8 for distances ranging from 1mm to 10mm.

In addition, error probabilities to occur are less in quaternary symbols than that in binary ones. Using both amplitude and phase shifting modulation will allow less use of amplitudes and thus fewer probabilities of errors.

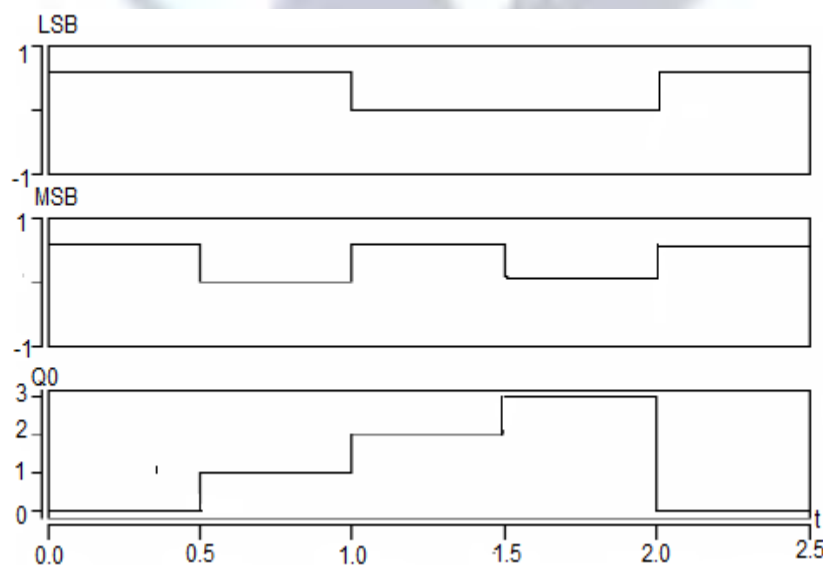


Figure 7: Quaternary to binary demodulator simulation

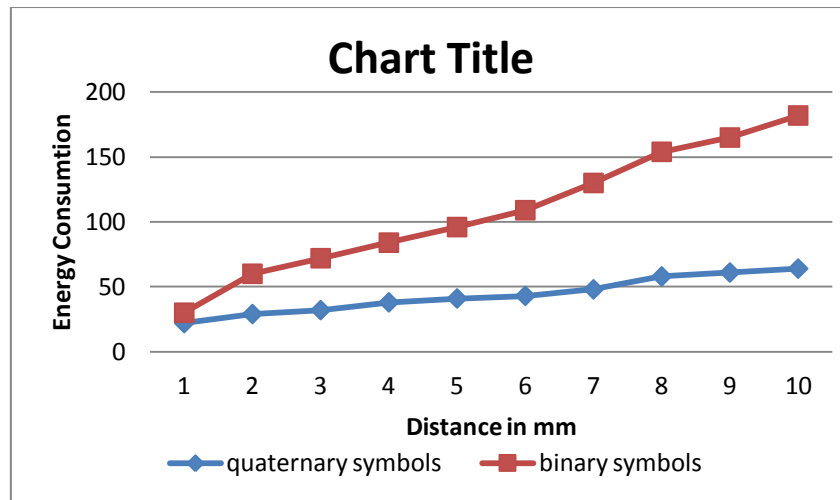


Figure 8: Energy consumption comparison between binary and quaternary transmitted symbols

V. CONCLUSION

A new Quaternary interconnect scheme is presented in this paper. The scheme modifies the transmission of data in a wireless sensor network from binary symbols to quaternary ones. Upon transmission each two bits will be modulated as one symbol, and upon reception the symbol will be demodulated producing the original binary bits. This scheme has been simulated with SPICE and the simulation results have shown that it can increase the life time of a WSN. The increase in life time is due to the decrease in the symbol rate for the same transmission rate. The savings in power consumption has been found to be 41% compared to binary transmission signaling schemes.

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